# 18-BIT, 580-kHz, UNIPOLAR INPUT, MICRO POWER SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH PARALLEL INTERFACE

## FEATURES

- 580-kHz Sample Rate
- 18-Bit NMC Ensured Over Temperature
- Zero Latency
- Low Power: 115 mW at 580 kHz
- Unipolar Input Range
- Onboard Reference Buffer and Conversion Clock
- Wide Buffer Supply, 2.7 V to 5.25 V
- Flexible 8-/16-/18-Bit Parallel Interface
- Pin Compatible With ADS8383
- 48-Pin TQFP Package

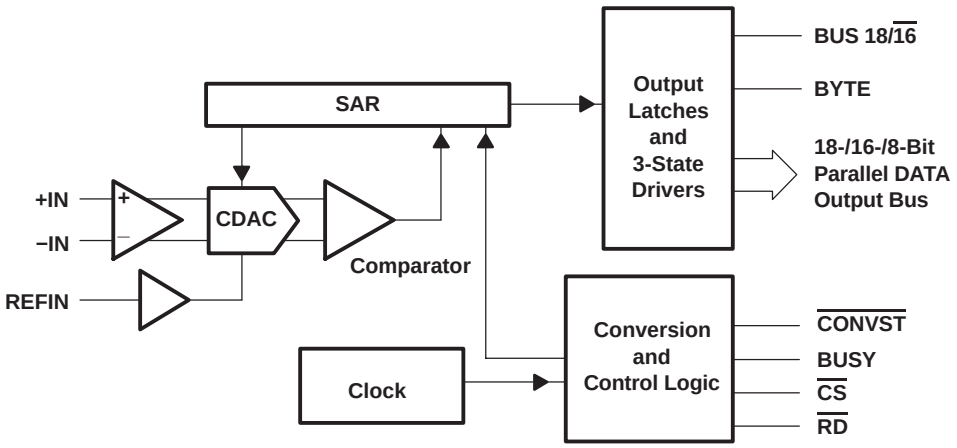
## APPLICATIONS

- Medical Instruments
- Optical Networking
- Transducer Interface
- High Accuracy Data Acquisition Systems
- Magnetometers

## DESCRIPTION

The ADS8381 is an 18-bit, 580 kHz A/D converter. The device includes a 18-bit capacitor-based SAR A/D converter with inherent sample and hold. The ADS8381 offers a full 18-bit interface, a 16-bit option where data is read using two read cycles, or an 8-bit bus option using three read cycles.

The ADS8381 is available in a 48-lead TQFP package and is characterized over the industrial −40°C to 85°C temperature range.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

| MODEL | MAXIMUM INTEGRAL LINEARITY (LSB) | MAXIMUM DIFFERENTIAL LINEARITY (LSB) | NO MISSING CODES RESOLUTION (BIT) | PACKAGE TYPE | PACKAGE DESIGNATOR | TEMPERATURE RANGE | ORDERING INFORMATION | TRANSPORT MEDIA QUANTITY |
|---|---|---|---|---|---|---|---|---|
| ADS8381I | ±6 | −2/3 | 17 | 48 Pin TQFP | PFB | −40°C to 85°C | ADS8381IPFBT | Tape and reel 250 |
| | | | | | | | ADS8381IPFBR | Tape and reel 1000 |
| ADS8381IB | ±5 | −1/2 | 18 | 48 Pin TQFP | PFB | −40°C to 85°C | ADS8381IBPFBT | Tape and reel 250 |
| | | | | | | | ADS8381IBPFBR | Tape and reel 1000 |

NOTE: For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

| | | UNIT |
|---|---|---|
| Voltage | +IN to AGND | −0.4 V to +VA + 0.1 V |
| | −IN to AGND | −0.4 V to 0.5 V |
| Voltage range | +VA to AGND | −0.3 V to 7 V |
| | +VBD to BDGND | −0.3 V to 7 V |
| | +VA to +VBD | −0.3 V to 2.55 V |
| Digital input voltage to BDGND | | −0.3 V to +VBD + 0.3 V |
| Digital output voltage to BDGND | | −0.3 V to +VBD + 0.3 V |
| Operating free-air temperature range, $T_A$ | | −40°C to 85°C |
| Storage temperature range, $T_{stg}$ | | −65°C to 150°C |
| Junction temperature ($T_J$ max) | | 150°C |
| TQFP package | Power dissipation | $(T_J Max - T_A)/\theta_{JA}$ |
| | $\theta_{JA}$ thermal impedance | 86°C/W |
| Lead temperature, soldering | Vapor phase (60 sec) | 215°C |
| | Infrared (15 sec) | 220°C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## SPECIFICATIONS

$T_A$ = −40°C to 85°C, +VA = 5 V, +VBD = 3 V or 5 V, $V_{ref}$ = 4.096 V, $f_{SAMPLE}$ = 580 kHz (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | ADS8381IB | | | ADS8381I | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **Analog Input** | | | | | | | | |
| Full-scale input voltage (see Note 1) | +IN − −IN | 0 | | $V_{ref}$ | 0 | | $V_{ref}$ | V |
| Absolute input voltage | +IN | −0.2 | | $V_{ref}$ + 0.2 | −0.2 | | $V_{ref}$ + 0.2 | V |
| | −IN | −0.2 | | 0.2 | −0.2 | | 0.2 | |
| Input capacitance | | | 45 | | | 45 | | pF |
| Input leakage current | | | 1 | | | 1 | | nA |
| **System Performance** | | | | | | | | |
| Resolution | | | 18 | | | 18 | | Bits |
| No missing codes | | 18 | | | 17 | | | Bits |
| Integral linearity (see Notes 2 and 3) | < 0.125 FS | −4 | −2.2/1 | 4 | −5 | | 5 | LSB (18 bit) |
| | > 0.125 FS | −5 | −3/2 | 5 | −6 | | 6 | |
| Differential linearity | | −1 | −0.6/1.25 | 2 | −2 | | 3 | LSB (18 bit) |
| Offset error | | −0.75 | ±0.25 | 0.75 | −1 | ±0.5 | 1 | mV |
| Gain error (see Note 4) | | −0.075 | | 0.075 | −0.1 | | 0.1 | %FS |
| Noise | | | 60 | | | 60 | | µV RMS |
| Power supply rejection ratio | At 3FFFFh output code | | 75 | | | 75 | | dB |
| **Sampling Dynamics** | | | | | | | | |
| Conversion time | | | | 1.4 | | | 1.4 | µs |
| Acquisition time | | 0.3 | | | 0.3 | | | µs |
| Throughput rate | | | | 580 | | | 580 | kHz |
| Aperture delay | | | 4 | | | 4 | | ns |
| Aperture jitter | | | 15 | | | 15 | | ps |
| Step response | | | 150 | | | 150 | | ns |
| Over voltage recovery | | | 150 | | | 150 | | ns |

(1) Ideal input span, does not include gain or offset error.
(2) LSB means least significant bit
(3) This is endpoint INL, not best fit.
(4) Measured relative to an ideal full-scale input (+IN − −IN) of 4.096 V

## SPECIFICATIONS (CONTINUED)

$T_A$ = −40°C to 85°C, +VA = +5 V, +VBD = 3 V or 5 V, $V_{ref}$ = 4.096 V, $f_{SAMPLE}$ = 580 kHz (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | ADS8381IB | | | ADS8381I | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | UNIT |
| **Dynamic Characteristics** | | | | | | | | |
| Total harmonic distortion (THD) (see Note 1) | 1 kHz | | −112 | | | −110 | | dB |
| | 10 kHz | | −106 | | | −100 | | |
| | 50 kHz | | −98 | | | −95 | | |
| | 100 kHz | | −95 | | | −90 | | |
| Signal to noise ratio (SNR) (see Note 1) | 1 kHz | | 88 | | | 87 | | dB |
| | 10 kHz | | 88 | | | 87 | | |
| | 50 kHz | | 88 | | | 87 | | |
| | 100 kHz | | 88 | | | 87 | | |
| Signal to noise + distortion (SINAD) (see Note 1) | 1 kHz | | 88 | | | 87 | | dB |
| | 10 kHz | | 88 | | | 87 | | |
| | 50 kHz | | 87 | | | 86 | | |
| | 100 kHz | | 87 | | | 86 | | |
| Spurious free dynamic range (SFDR) (see Note 1) | 1 kHz | | 113 | | | 112 | | dB |
| | 10 kHz | | 108 | | | 98 | | |
| | 50 kHz | | 99 | | | 96 | | |
| | 100 kHz | | 97 | | | 90 | | |
| −3dB Small signal bandwidth | | | 3 | | | 3 | | MHz |
| **Voltage Reference Input** | | | | | | | | |
| Reference voltage at REFIN, $V_{ref}$ | | 2.5 | 4.096 | 4.2 | 2.5 | 4.096 | 4.2 | V |
| Reference resistance (see Note 2) | | | 500 | | | 500 | | kΩ |
| Reference current drain | $f_S$ = 580 kHz | | | 1 | | | 1 | mA |

(1) Calculated on the first nine harmonics of the input frequency
(2) Can vary ±20%

## SPECIFICATIONS (CONTINUED)

$T_A$ = −40°C to 85°C, +VA = +5 V, +VBD = 3 V or 5 V, $V_{ref}$ = 4.096 V, $f_{SAMPLE}$ = 580 kHz (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Digital Input/Output** | | | | | | |
| Logic family | | | | CMOS | | |
| Logic level | $V_{IH}$ | $I_{IH}$ = 5 µA | +VBD−1 | | $+V_{BD}$ + 0.3 | V |
| | $V_{IL}$ | $I_{IL}$ = 5 µA | −0.3 | | 0.8 | |
| | $V_{OH}$ | $I_{OH}$ = 2 TTL loads | $+V_{BD}$ − 0.6 | | | |
| | $V_{OL}$ | $I_{OL}$ = 2 TTL loads | | | 0.4 | |
| Data format | | | | Straight Binary | | |
| **Power Supply Requirements** | | | | | | |
| Power supply voltage | +VBD Buffer supply | | 2.7 | 3.3 | 5.25 | V |
| | +VA Analog supply | | 4.75 | 5 | 5.25 | V |
| Supply current, 580-kHz sample rate (see Note 1) | | | | 23 | 26 | mA |
| Power dissipation, 580-kHz sample rate (see Note 1) | | | | 115 | 130 | mW |
| **Temperature Range** | | | | | | |
| Operating free-air | | | −40 | | 85 | °C |

(1) This includes only +VA current. +VBD current is typical 1 mA with 5 pF load capacitance on all output pins.

## TIMING CHARACTERISTICS

All specifications typical at −40°C to 85°C, +VA = +VBD = 5 V (see Notes 1, 2, and 3)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{CONV}$ | Conversion time | | | 1.4 | µs |
| $t_{ACQ}$ | Acquisition time | 0.3 | | | µs |
| $t_{HOLD}$ | Sampling capacitor hold time | | | 25 | ns |
| $t_{pd1}$ | $\overline{CONVST}$ low to conversion started (BUSY high) | | | 45 | ns |
| $t_{pd2}$ | Propagation delay time, End of conversion to BUSY low | | | 20 | ns |
| $t_{pd3}$ | Propagation delay time, from start of conversion (internal state) to rising edge of BUSY | | | 20 | ns |
| $t_{w1}$ | Pulse duration, $\overline{CONVST}$ low | 40 | | 600 | ns |
| $t_{su1}$ | Setup time, $\overline{CS}$ low to $\overline{CONVST}$ low | 20 | | | ns |
| $t_{w2}$ | Pulse duration, $\overline{CONVST}$ high | 20 | | | ns |
| | $\overline{CONVST}$ falling edge jitter | | | 10 | ps |
| $t_{w3}$ | Pulse duration, BUSY signal low | Min($t_{ACQ}$) | | | µs |
| $t_{w4}$ | Pulse duration, BUSY signal high | | | 1.4 | µs |
| $t_{h1}$ | Hold time, First data bus data transition ($\overline{CS}$ low for read cycle, or $\overline{RD}$ or BYTE or BUS18/$\overline{16}$ input changes) after $\overline{CONVST}$ low | 40 | | 600 | ns |
| $t_{d1}$ | Delay time, $\overline{CS}$ low to $\overline{RD}$ low | 0 | | | ns |
| $t_{su2}$ | Setup time, $\overline{RD}$ high to $\overline{CS}$ high | 0 | | | ns |
| $t_{w5}$ | Pulse duration, $\overline{RD}$ low time | 50 | | | ns |
| $t_{en}$ | Enable time, $\overline{RD}$ low (or $\overline{CS}$ low for read cycle) to data valid | | | 20 | ns |
| $t_{d2}$ | Delay time, data hold from $\overline{RD}$ high | 5 | | | ns |
| $t_{d3}$ | Delay time, BUS18/$\overline{16}$ or BYTE rising edge or falling edge to data valid | 10 | | 20 | ns |
| $t_{w6}$ | Pulse duration, $\overline{RD}$ high | 20 | | | ns |
| $t_{w7}$ | Pulse duration, $\overline{CS}$ high time | 20 | | | ns |
| $t_{h2}$ | Hold time, last $\overline{CS}$ rising edge or changes of $\overline{RD}$, BYTE, or BUS18/$\overline{16}$ to $\overline{CONVST}$ falling edge | 125 | | | ns |
| $t_{pd4}$ | Propagation delay time, BUSY falling edge to next $\overline{RD}$ (or $\overline{CS}$ for read cycle) falling edge | Max($t_{d5}$) | | | ns |
| $t_{d4}$ | Delay time, BYTE edge to BUS18/$\overline{16}$ edge skew | 0 | | | ns |
| $t_{su3}$ | Setup time, BYTE or BUS18/$\overline{16}$ transition to $\overline{RD}$ falling edge | 10 | | | ns |
| $t_{h3}$ | Hold time, BYTE or BUS18/$\overline{16}$ transition to $\overline{RD}$ falling edge | 10 | | | ns |
| $t_{dis}$ | Disable time, $\overline{RD}$ High ($\overline{CS}$ high for read cycle) to 3-stated data bus | | | 20 | ns |
| $t_{d5}$ | Delay time, BUSY low to MSB data valid | | | 30 | ns |
| $t_{su5}$ | Setup time, BYTE transition to next BYTE transition, or BUS18/$\overline{16}$ transition to next BUS18/$\overline{16}$ transition | 50 | | | ns |
| $t_{su(AB)}$ | Setup time, from the falling edge of $\overline{CONVST}$ (used to start the valid conversion) to the next falling edge of $\overline{CONVST}$ (when $\overline{CS}$ = 0 and $\overline{CONVST}$ used to abort) or to the next falling edge of $\overline{CS}$ (when $\overline{CS}$ is used to abort). | 65 | | 1000 | ns |
| $t_{f(\overline{CONVST})}$ | Falling time, ($\overline{CONVST}$ falling edge) | 10 | | 30 | ns |
| $t_{su6}$ | Setup time, $\overline{CS}$ falling edge to $\overline{CONVST}$ falling edge when $\overline{RD}$ = 0 | 125 | | | ns |

(1) All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$ except for $\overline{CONVST}$.
(2) See timing diagrams.
(3) All timing are measured with 20 pF equivalent loads on all data bits and BUSY pins.

## TIMING CHARACTERISTICS

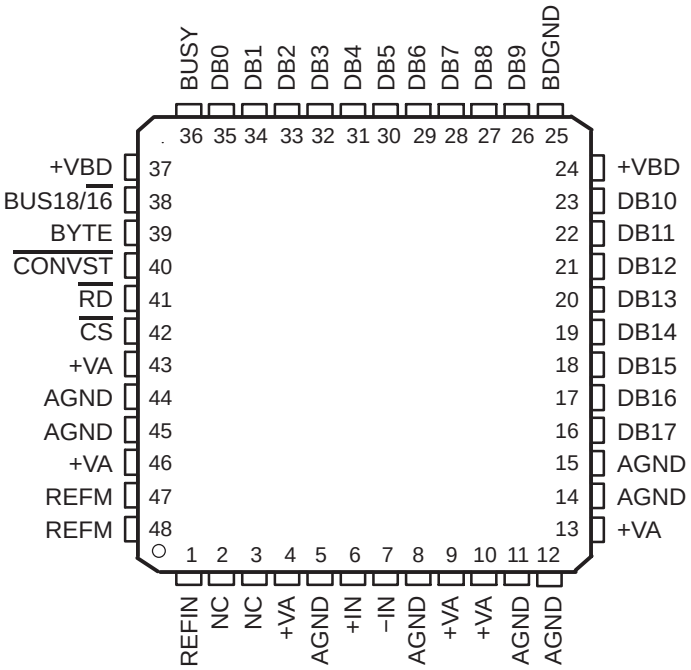
All specifications typical at −40°C to 85°C, +VA = 5 V, +VBD = 3 V (see Notes 1, 2, and 3)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{CONV}$ | Conversion time | | | 1.4 | µs |
| $t_{ACQ}$ | Acquisition time | 0.3 | | | µs |
| $t_{HOLD}$ | Sampling capacitor hold time | | | 25 | ns |
| $t_{pd1}$ | $\overline{CONVST}$ low to conversion started (BUSY high) | | | 50 | ns |
| $t_{pd2}$ | Propagation delay time, end of conversion to BUSY low | | | 25 | ns |
| $t_{pd3}$ | Propagation delay time, from start of conversion (internal state) to rising edge of BUSY | | | 25 | ns |
| $t_{w1}$ | Pulse duration, $\overline{CONVST}$ low | 40 | | 600 | ns |
| $t_{su1}$ | Setup time, $\overline{CS}$ low to $\overline{CONVST}$ low | 20 | | | ns |
| $t_{w2}$ | Pulse duration, $\overline{CONVST}$ high | 20 | | | ns |
| | $\overline{CONVST}$ falling edge jitter | | | 10 | ps |
| $t_{w3}$ | Pulse duration, BUSY signal low | Min($t_{ACQ}$) | | | µs |
| $t_{w4}$ | Pulse duration, BUSY signal high | | | 1.4 | µs |
| $t_{h1}$ | Hold time, first data bus transition ($\overline{CS}$ low for read cycle, or $\overline{RD}$ or BYTE or BUS 18/$\overline{16}$ input changes) after $\overline{CONVST}$ low | 40 | | 600 | ns |
| $t_{d1}$ | Delay time, $\overline{CS}$ low to $\overline{RD}$ low | 0 | | | ns |
| $t_{su2}$ | Setup time, $\overline{RD}$ high to $\overline{CS}$ high | 0 | | | ns |
| $t_{w5}$ | Pulse duration, $\overline{RD}$ low | 50 | | | ns |
| $t_{en}$ | Enable time, $\overline{RD}$ low (or $\overline{CS}$ low for read cycle) to data valid | | | 30 | ns |
| $t_{d2}$ | Delay time, data hold from $\overline{RD}$ high | 10 | | | ns |
| $t_{d3}$ | Delay time, BUS18/$\overline{16}$ or BYTE rising edge or falling edge to data valid | 10 | | 30 | ns |
| $t_{w6}$ | Pulse duration, $\overline{RD}$ high time | 20 | | | ns |
| $t_{w7}$ | Pulse duration, $\overline{CS}$ high time | 20 | | | ns |
| $t_{h2}$ | Hold time, last $\overline{CS}$ rising edge or changes of $\overline{RD}$, BYTE, or BUS18/$\overline{16}$ to $\overline{CONVST}$ falling edge | 125 | | | ns |
| $t_{pd4}$ | Propagation delay time, BUSY falling edge to next $\overline{RD}$ (or $\overline{CS}$ for read cycle) falling edge | Max(td5) | | | ns |
| $t_{d4}$ | Delay time, BYTE edge to BUS18/$\overline{16}$ edge skew | 0 | | | ns |
| $t_{su3}$ | Setup time, BYTE or BUS18/$\overline{16}$ transition to $\overline{RD}$ falling edge | 10 | | | ns |
| $t_{h3}$ | Hold time, BYTE or BUS18/$\overline{16}$ transition to $\overline{RD}$ falling edge | 10 | | | ns |
| $t_{dis}$ | Disable time, $\overline{RD}$ High ($\overline{CS}$ high for read cycle) to 3-stated data bus | | | 30 | ns |
| $t_{d5}$ | Delay time, BUSY low to MSB data valid delay time | | | 40 | ns |
| $t_{su5}$ | Setup time, BYTE transition to next BYTE transition, or BUS18/$\overline{16}$ transition to next BUS18/$\overline{16}$ transition | 50 | | | ns |
| $t_{su(AB)}$ | Setup time, from the falling edge of $\overline{CONVST}$ (used to start the valid conversion) to the next falling edge of $\overline{CONVST}$ (when $\overline{CS}$ = 0 and $\overline{CONVST}$ used to abort) or to the next falling edge of $\overline{CS}$ (when $\overline{CS}$ is used to abort). | 70 | | 1000 | ns |
| $t_{f(\overline{CONVST})}$ | Falling time, ($\overline{CONVST}$ falling edge) | 10 | | 30 | ns |
| $t_{su6}$ | Setup time, $\overline{CS}$ falling edge to $\overline{CONVST}$ falling edge when $\overline{RD}$ = 0 | 125 | | | ns |

(1) All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +VBD) and timed from a voltage level of ($V_{IL} + V_{IH}$)/2 except for $\overline{CONVST}$.
(2) See timing diagrams.
(3) All timing are measured with 10 pF equivalent loads on all data bits and BUSY pins.

## PIN ASSIGNMENTS

**PFB PACKAGE**
**(TOP VIEW)**




NC − No connection.

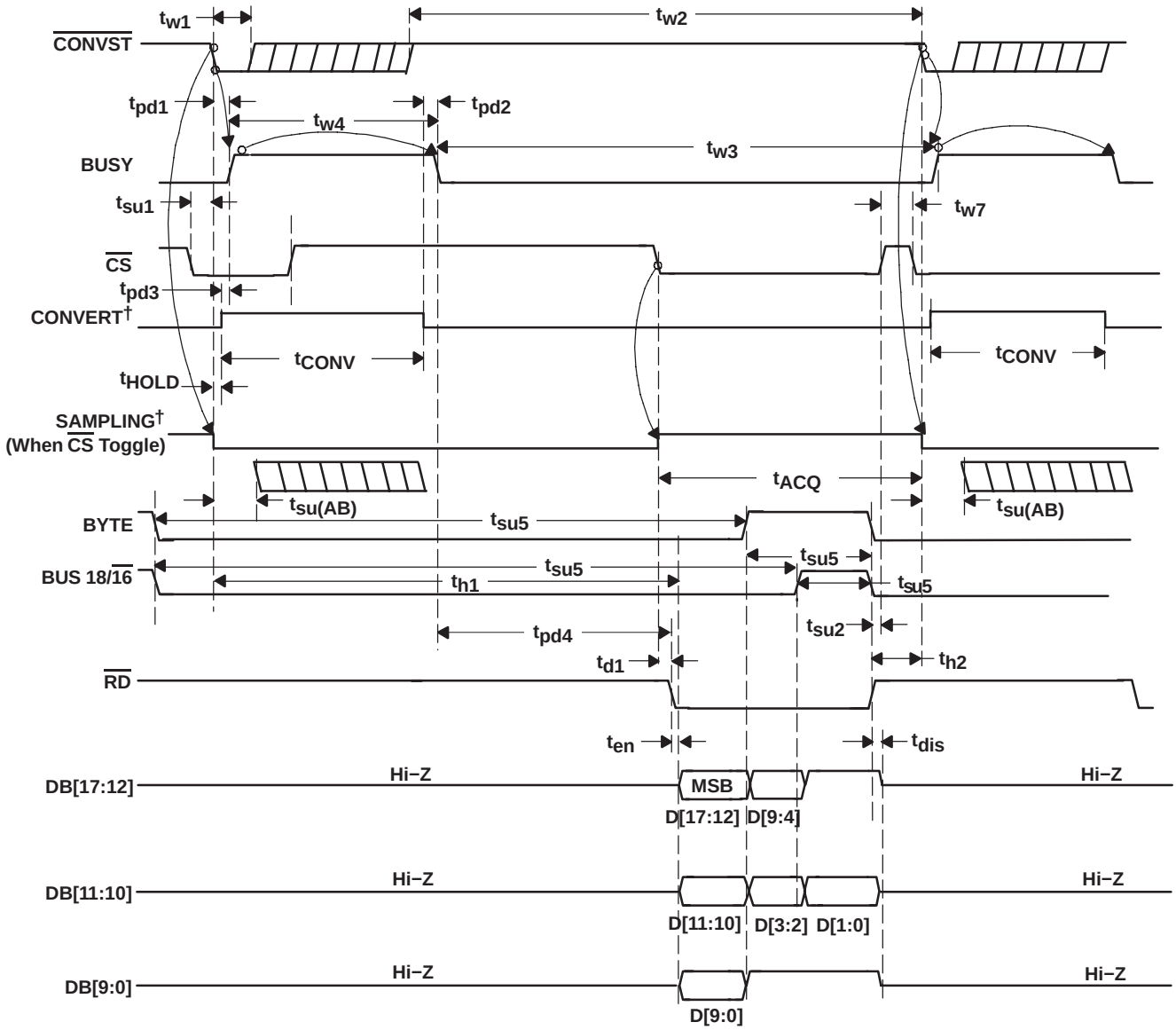
## TERMINAL FUNCTIONS

| NAME | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AGND | 5, 8, 11, 12, 14, 15, 44, 45 | − | Analog ground |
| BDGND | 25 | − | Digital ground for buffer supply |
| BUSY | 36 | O | Status output. High when a conversion is in progress. |
| BUS18/$\overline{16}$ | 38 | I | Bus size select input. Used for selecting 18-bit or 16-bit wide bus transfer.<br>0: Data bits output on the 18-bit data bus pins DB[17:0].<br>1: Last two data bits D[1:0] from 18-bit wide bus output on:<br>a) the low byte pins DB[9:2] if BYTE = 0<br>b) the high byte pins DB[17:10] if BYTE = 1 |
| BYTE | 39 | I | Byte select input. Used for 8-bit bus reading.<br>0: No fold back<br>1: Low byte D[9:2] of the 16 most significant bits is folded back to high byte of the 16 most significant pins DB[17:10]. |
| $\overline{\text{CONVST}}$ | 40 | I | Convert start. The falling edge of this input ends the acquisition period and starts the hold period. |
| $\overline{\text{CS}}$ | 42 | I | Chip select. The falling edge of this input starts the acquisition period. |

| Data Bus | | | 8-Bit Bus | | | 16-Bit Bus | | 18-Bit Bus |
|---|---|---|---|---|---|---|---|---|
| | | | BYTE = 0 | BYTE = 1 | BYTE = 1 | BYTE = 0 | BYTE = 0 | BYTE = 0 |
| | | | BUS18/$\overline{16}$ = 0 | BUS18/$\overline{16}$ = 0 | BUS18/$\overline{16}$ = 1 | BUS18/$\overline{16}$ = 0 | BUS18/$\overline{16}$ = 1 | BUS18/$\overline{16}$ = 0 |
| DB17 | 16 | O | D17 (MSB) | D9 | All ones | D17 (MSB) | All ones | D17 (MSB) |
| DB16 | 17 | O | D16 | D8 | All ones | D16 | All ones | D16 |
| DB15 | 18 | O | D15 | D7 | All ones | D15 | All ones | D15 |
| DB14 | 19 | O | D14 | D6 | All ones | D14 | All ones | D14 |
| DB13 | 20 | O | D13 | D5 | All ones | D13 | All ones | D13 |
| DB12 | 21 | O | D12 | D4 | All ones | D12 | All ones | D12 |
| DB11 | 22 | O | D11 | D3 | D1 | D11 | All ones | D11 |
| DB10 | 23 | O | D10 | D2 | D0(LSB) | D10 | All ones | D10 |
| DB9 | 26 | O | D9 | All ones | All ones | D9 | All ones | D9 |
| DB8 | 27 | O | D8 | All ones | All ones | D8 | All ones | D8 |
| DB7 | 28 | O | D7 | All ones | All ones | D7 | All ones | D7 |
| DB6 | 29 | O | D6 | All ones | All ones | D6 | All ones | D6 |
| DB5 | 30 | O | D5 | All ones | All ones | D5 | All ones | D5 |
| DB4 | 31 | O | D4 | All ones | All ones | D4 | All ones | D4 |
| DB3 | 32 | O | D3 | All ones | All ones | D3 | D1 | D3 |
| DB2 | 33 | O | D2 | All ones | All ones | D2 | D0 (LSB) | D2 |
| DB1 | 34 | O | D1 | All ones | All ones | D1 | All ones | D1 |
| DB0 | 35 | O | D0 (LSB) | All ones | All ones | D0 (LSB) | All ones | D0 (LSB) |

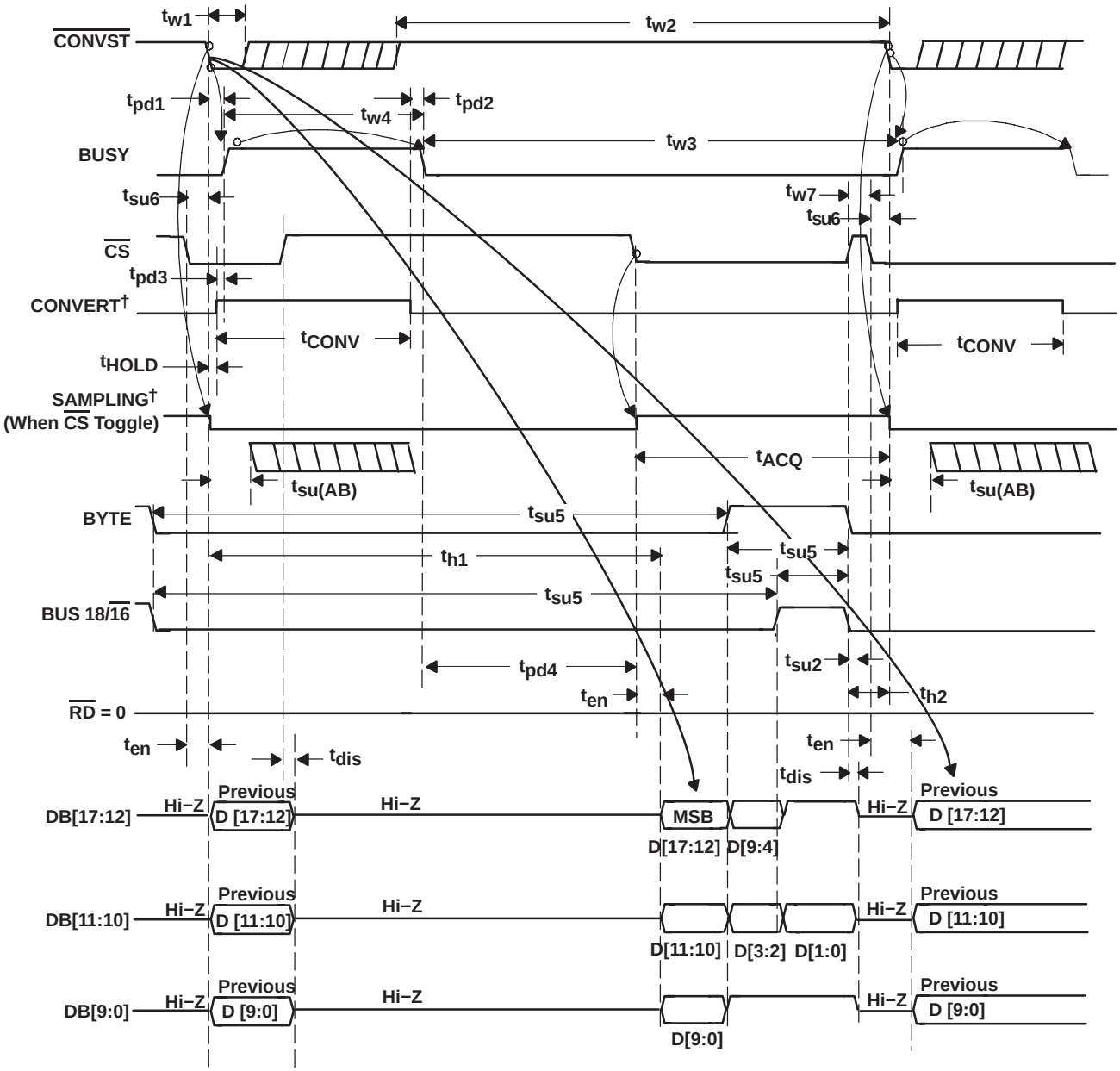
| | | | |
|---|---|---|---|
| −IN | 7 | I | Inverting input channel |
| +IN | 6 | I | Noninverting input channel |
| NC | 2, 3 | − | No connection |
| REFIN | 1 | I | Reference input. |
| REFM | 47, 48 | I | Reference ground. |
| $\overline{\text{RD}}$ | 41 | I | Synchronization pulse for the parallel output. When $\overline{\text{CS}}$ is low, this serves as the output enable and puts the previous conversion result on the bus. |
| +VA | 4, 9, 10, 13, 43, 46 | − | Analog power supplies, 5-V dc |
| +VBD | 24, 37 | − | Digital power supply for buffer |

## TIMING DIAGRAMS



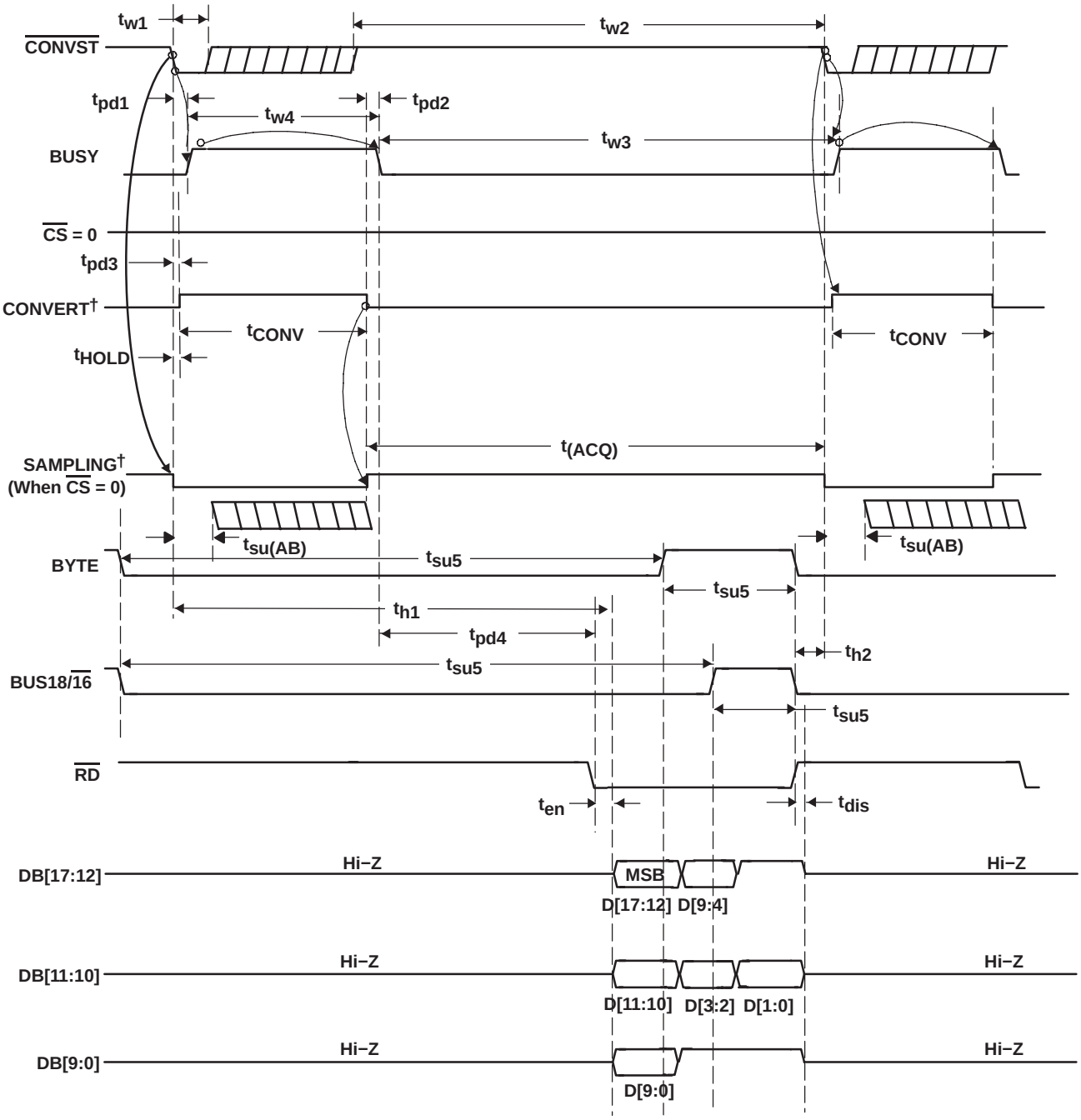

†Signal internal to device

**Figure 1. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ and $\overline{RD}$ Toggling**



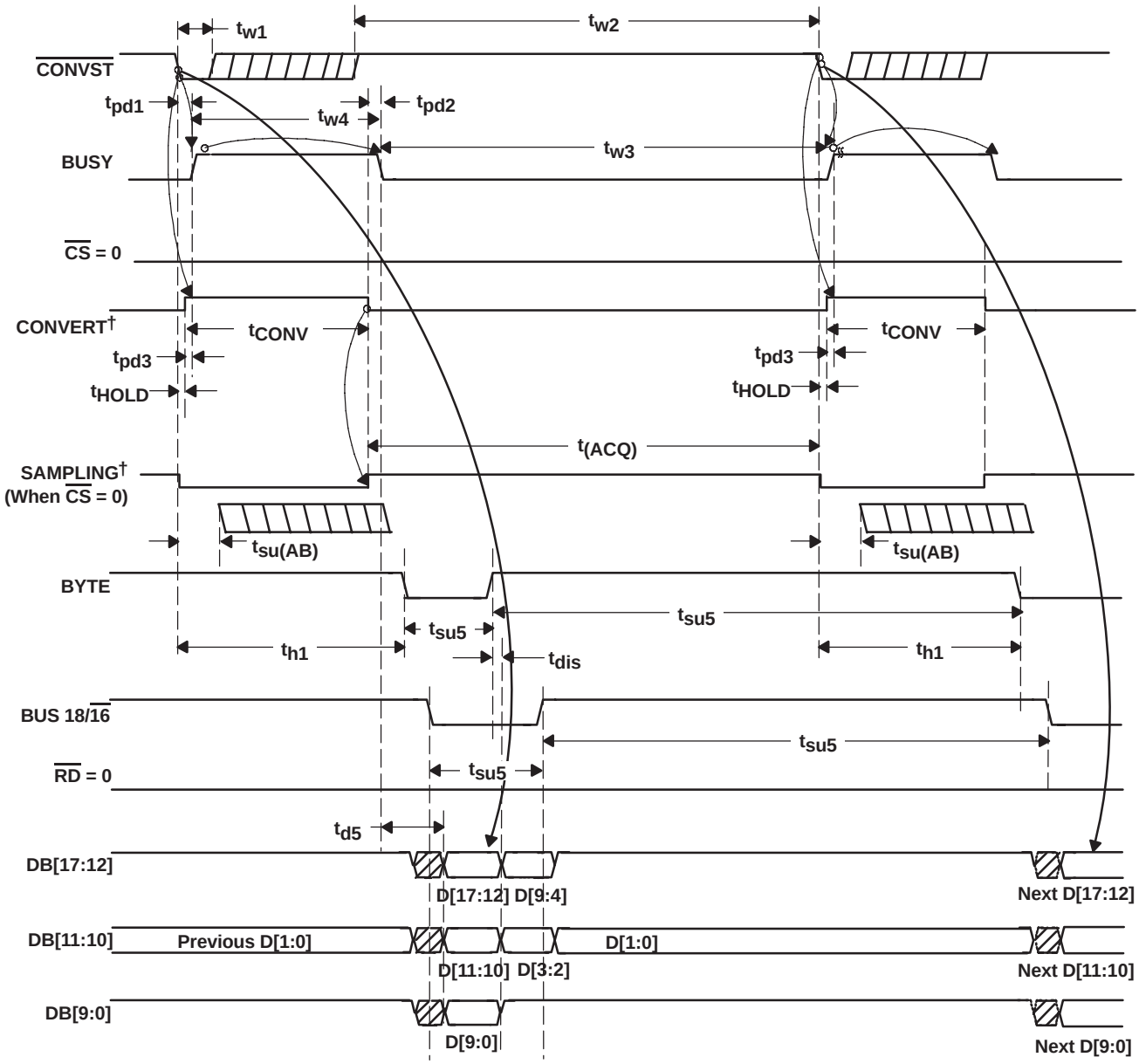

†Signal internal to device

**Figure 2. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ Toggling, $\overline{RD}$ Tied to BDGND**




†Signal internal to device

**Figure 3. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ Tied to BDGND, $\overline{RD}$ Toggling**




†Signal internal to device

**Figure 4. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ and $\overline{RD}$ Tied to BDGND—Auto Read**

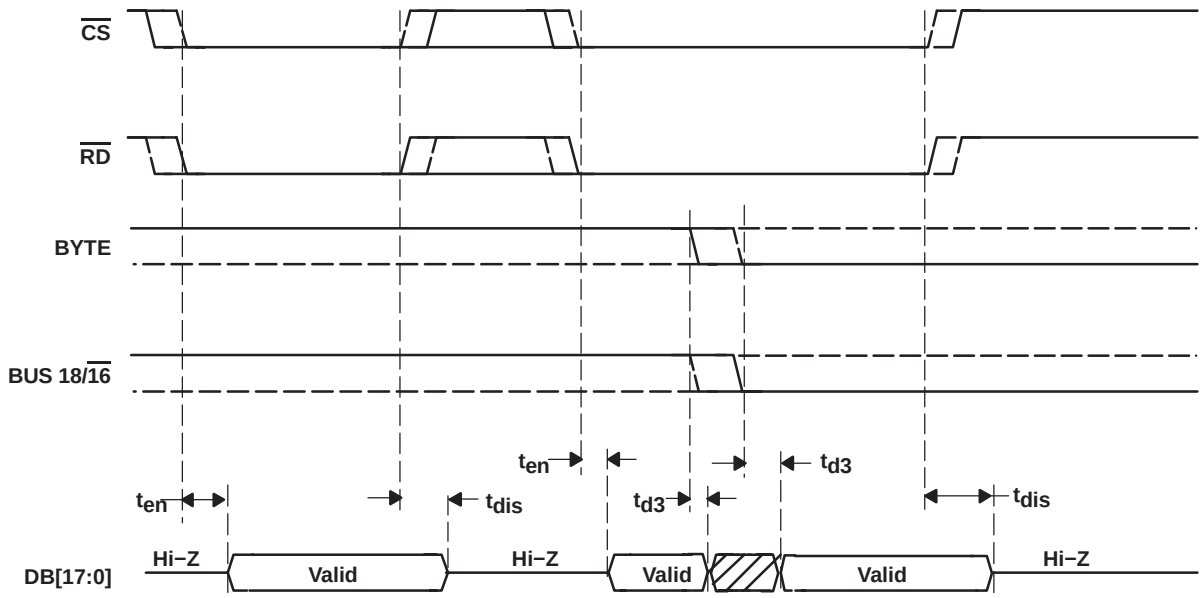



**Figure 5. Detailed Timing for Read Cycles**

## TYPICAL CHARACTERISTICS(1)

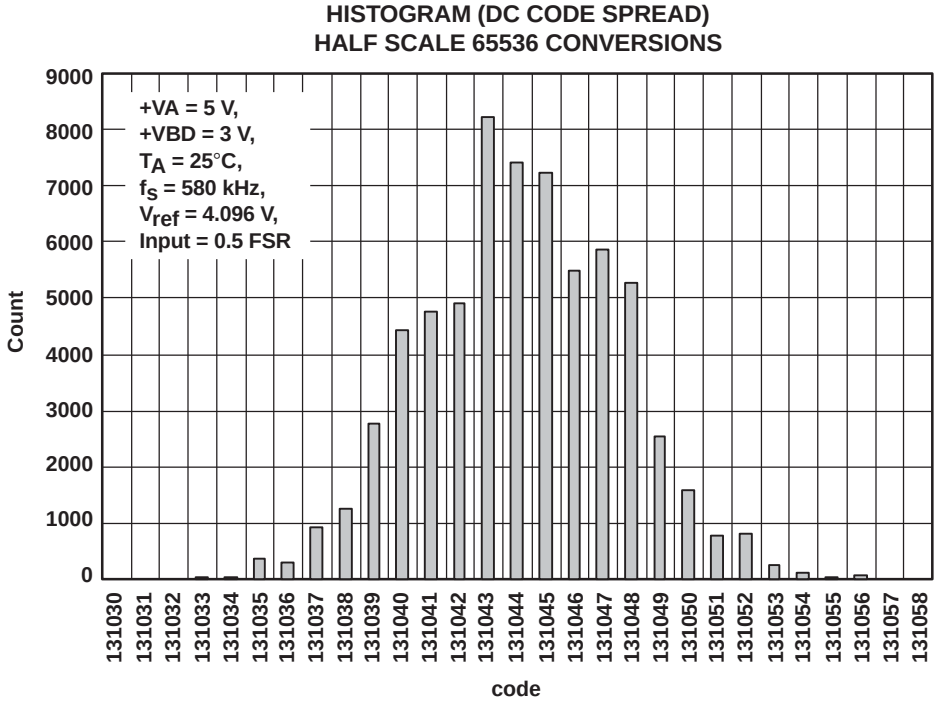



**Figure 6**

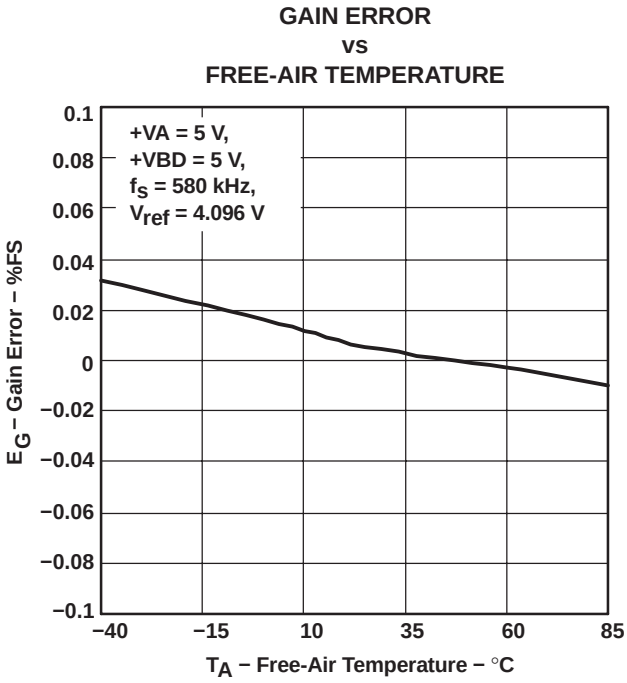



**Figure 7**

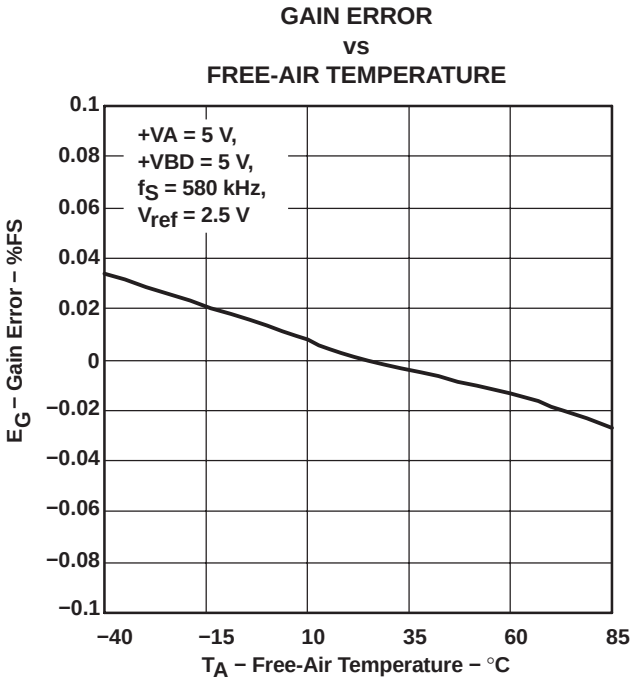



**Figure 8**

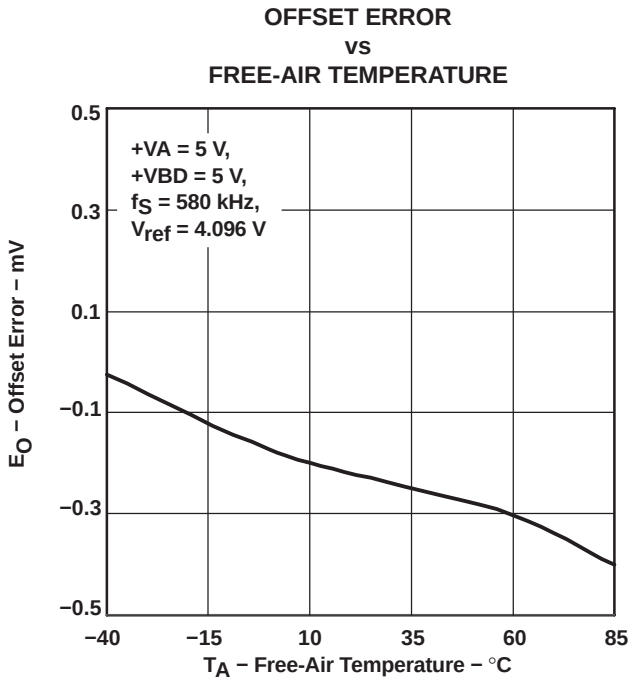



Figure 9

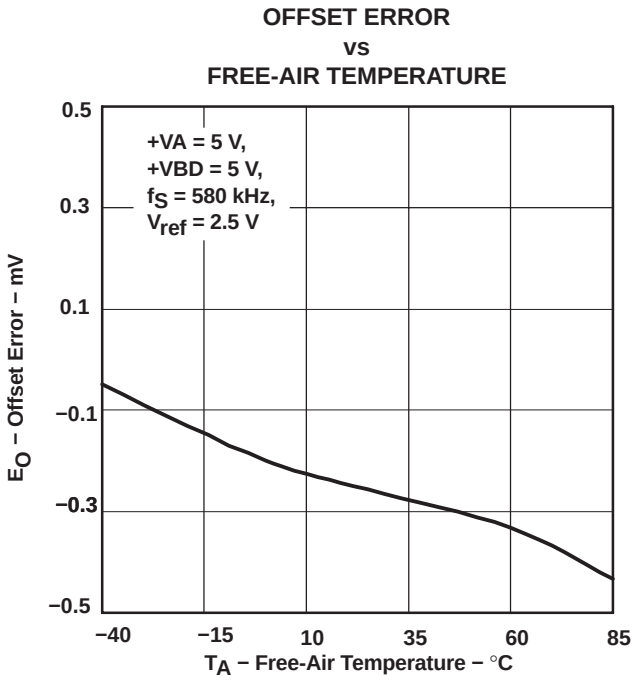



Figure 10

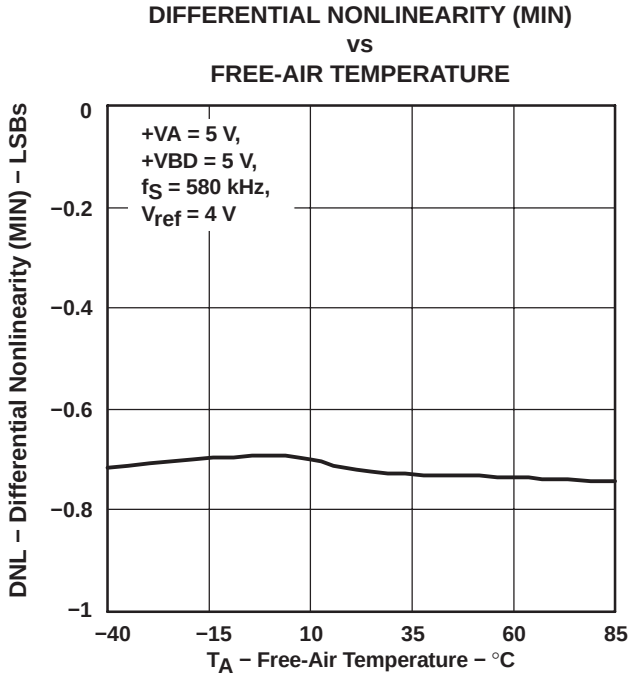



Figure 11

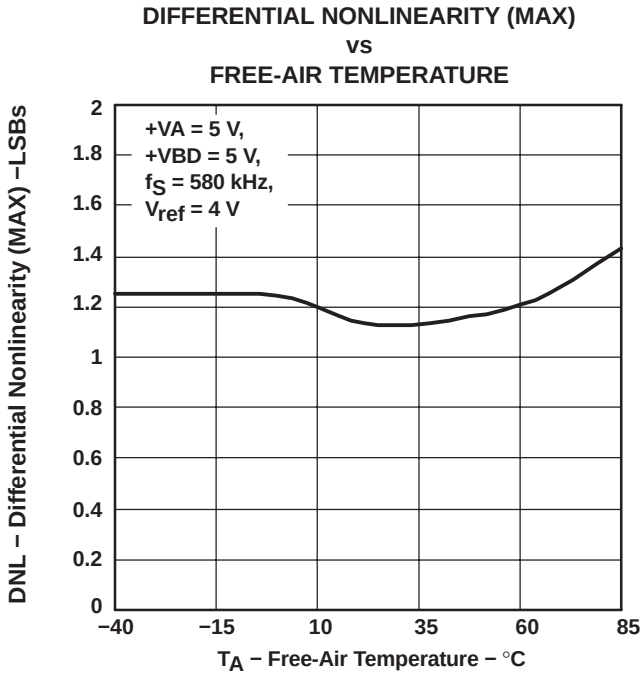



Figure 12

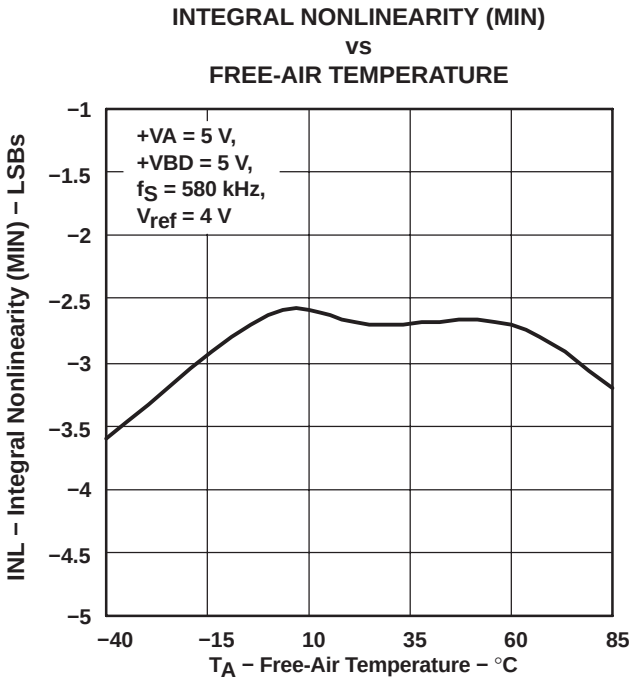



Figure 13

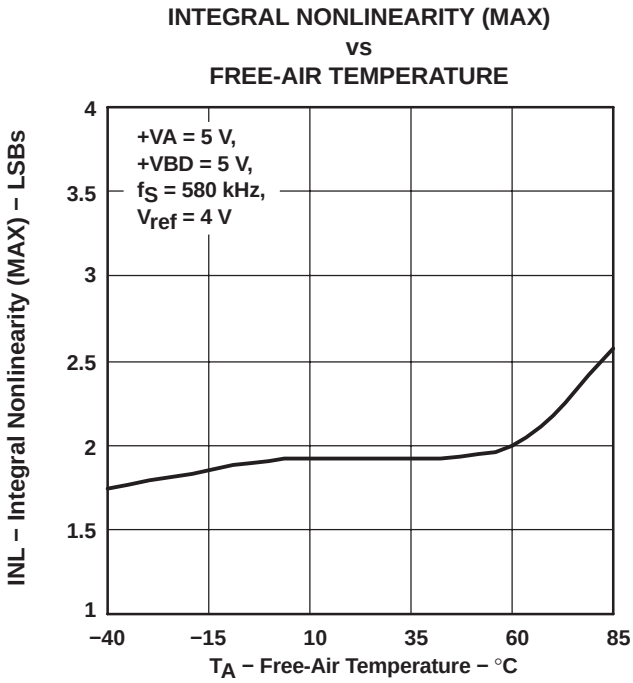



Figure 14

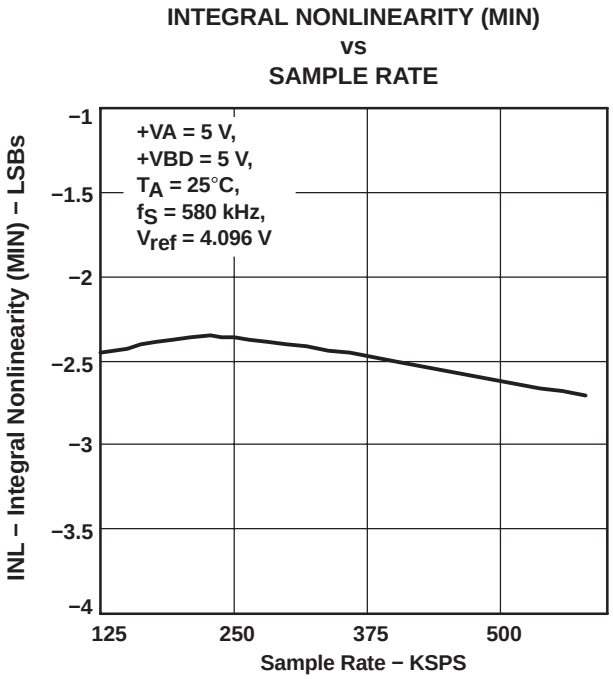



Figure 15

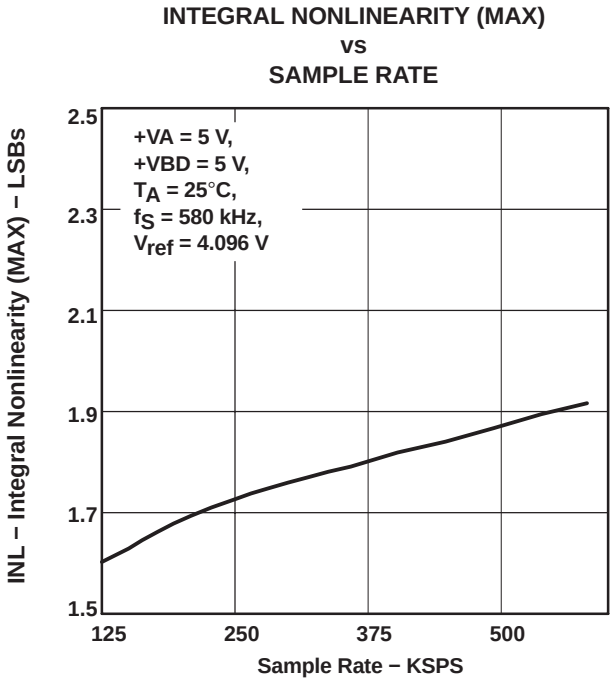



Figure 16

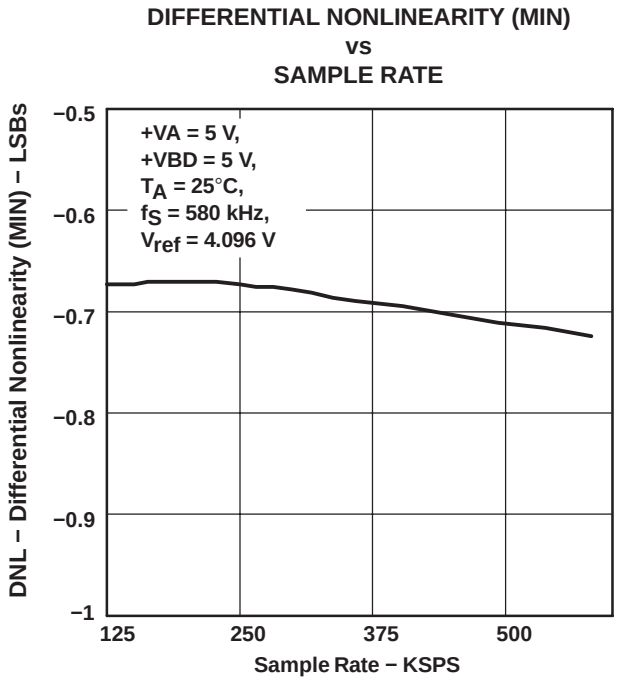



Figure 17

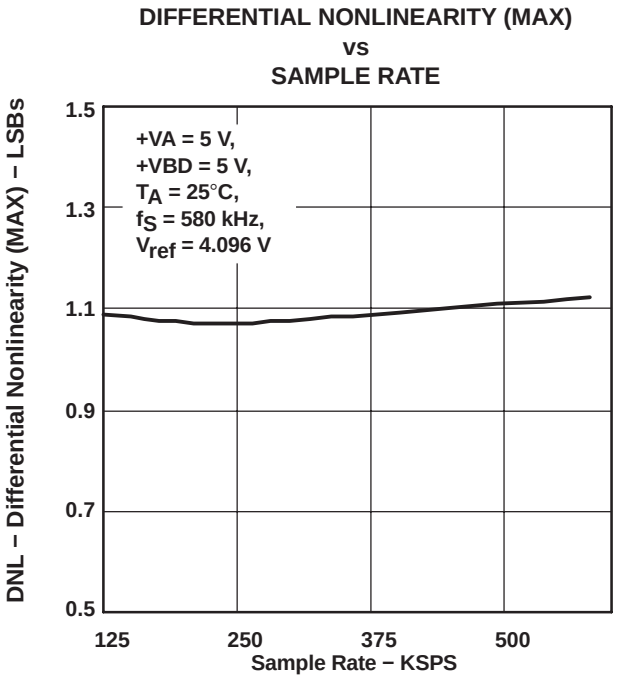



Figure 18

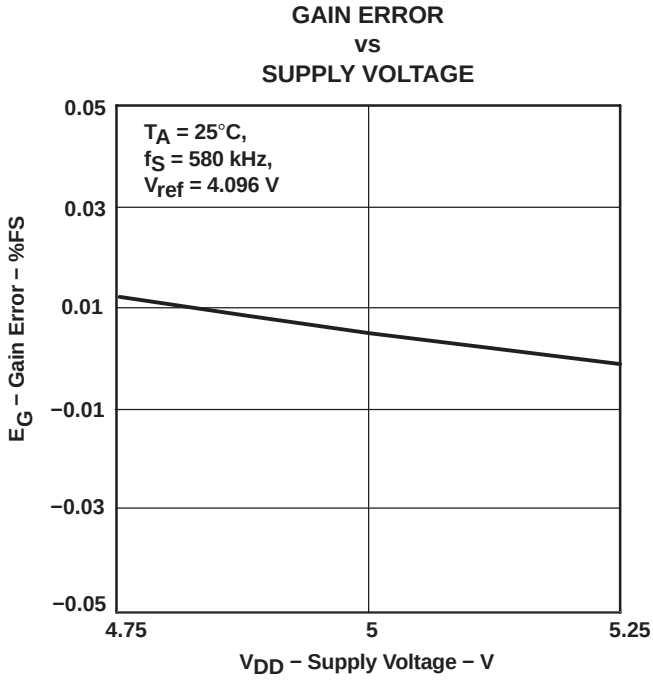



Figure 19

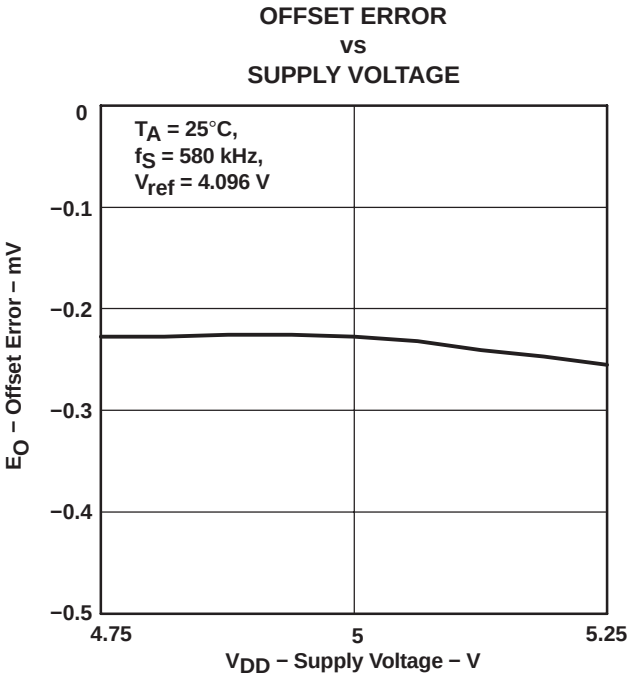



Figure 20

**+VA ANALOG SUPPLY CURRENT vs SUPPLY VOLTAGE**

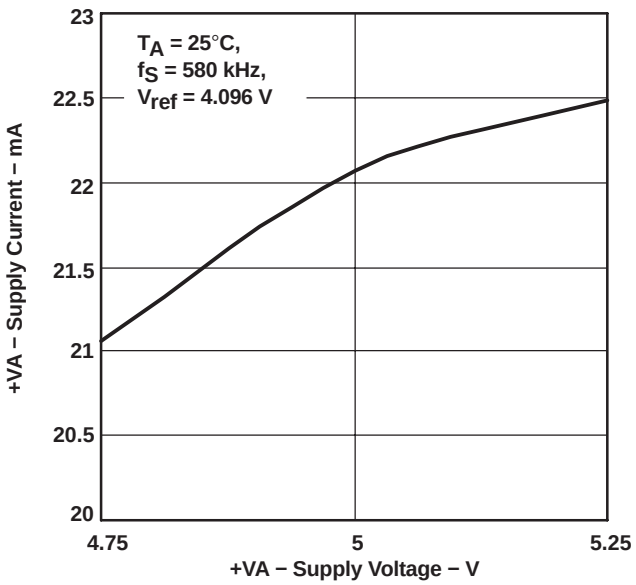



**Figure 21**

**DIFFERENTIAL NONLINEARITY (MIN) vs SUPPLY VOLTAGE**

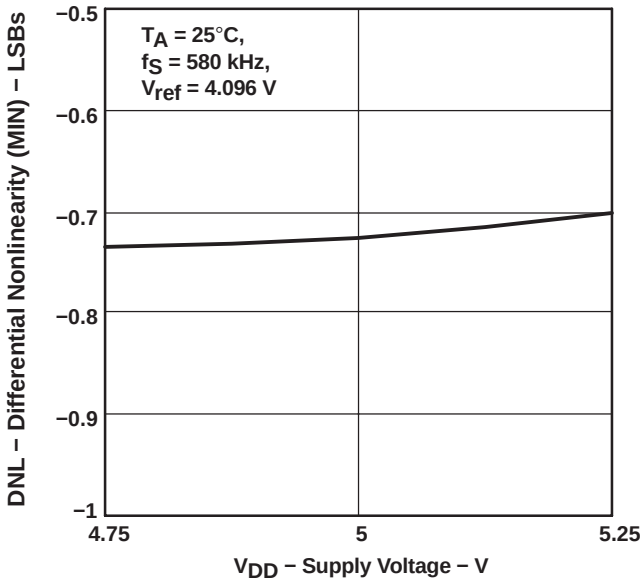



**Figure 22**

**DIFFERENTIAL NONLINEARITY (MAX) vs SUPPLY VOLTAGE**

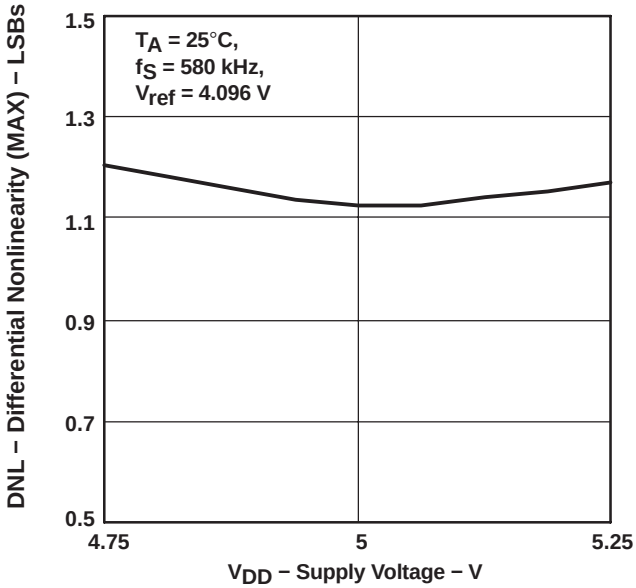



**Figure 23**

**INTEGRAL NONLINEARITY (MIN) vs SUPPLY VOLTAGE**

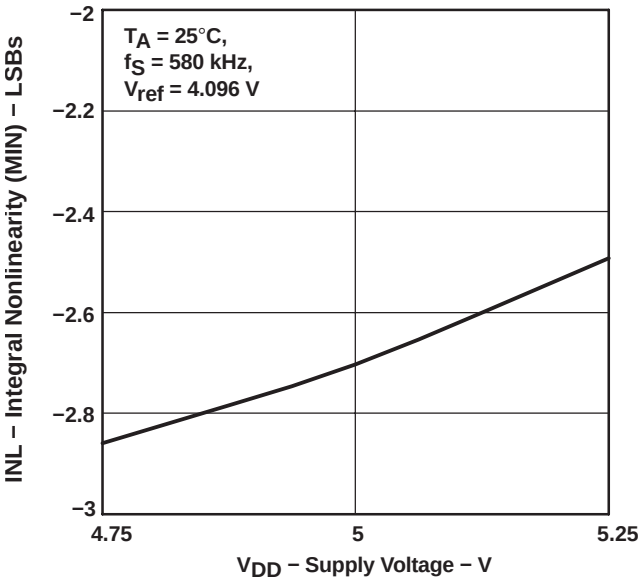



**Figure 24**

INTEGRAL NONLINEARITY (MAX)
vs
SUPPLY VOLTAGE

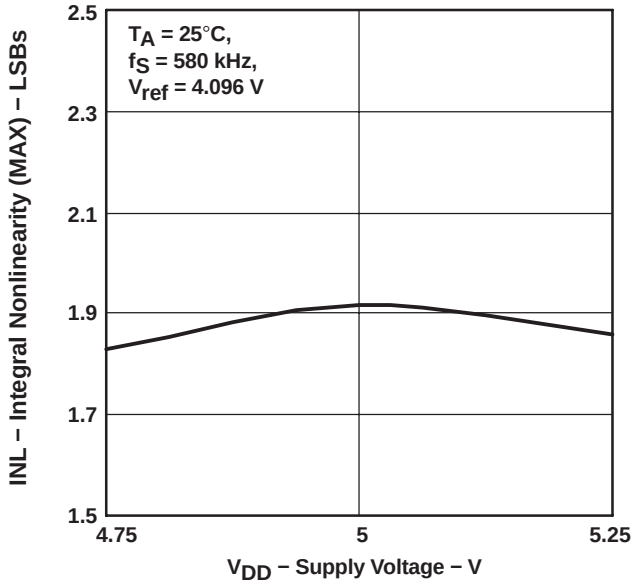



Figure 25

DIFFERENTIAL NONLINEARITY (MIN)
vs
REFERENCE VOLTAGE

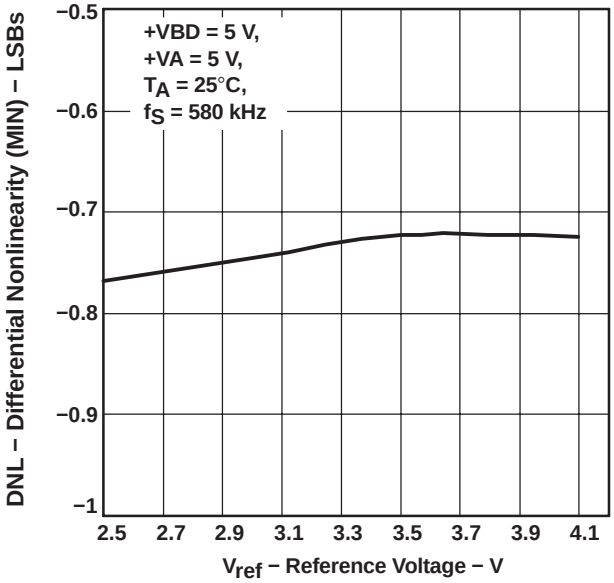



Figure 26

DIFFERENTIAL NONLINEARITY (MAX)
vs
REFERENCE VOLTAGE

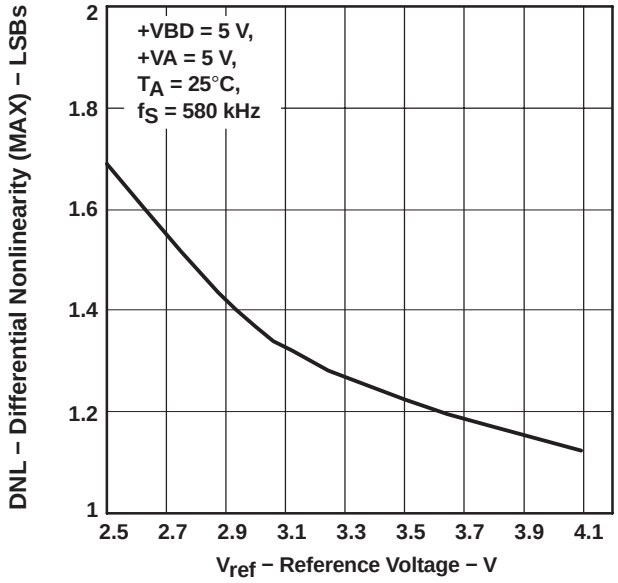



Figure 27

INTEGRAL NONLINEARITY (MIN)
vs
REFERENCE VOLTAGE

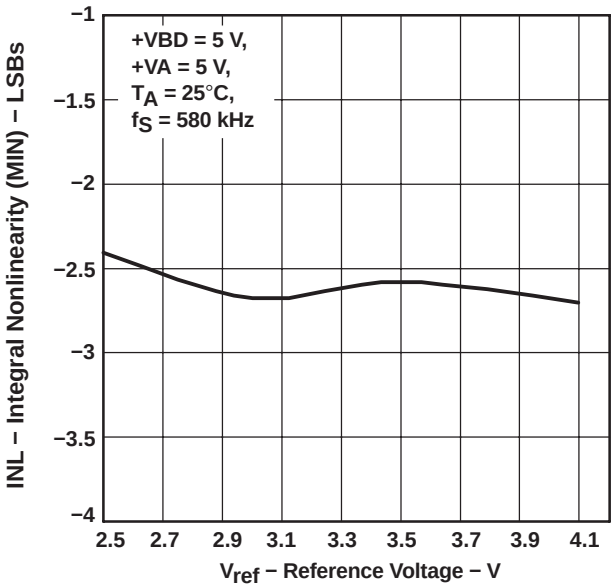



Figure 28

**INTEGRAL NONLINEARITY (MAX)**
**vs**
**REFERENCE VOLTAGE**

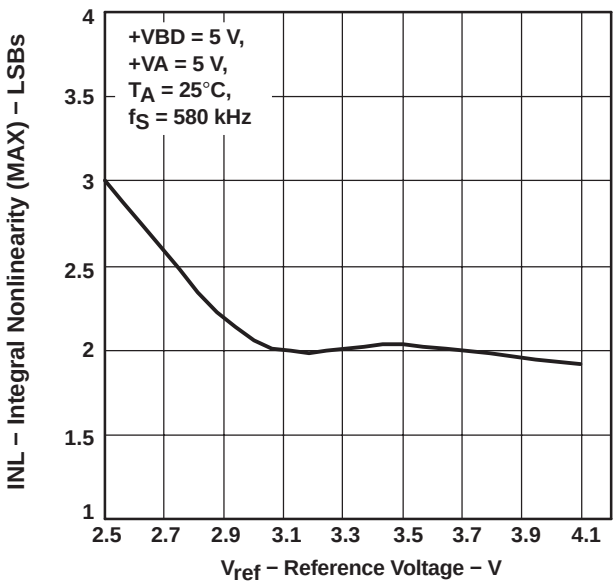



**Figure 29**

**OFFSET ERROR**
**vs**
**REFERENCE VOLTAGE**

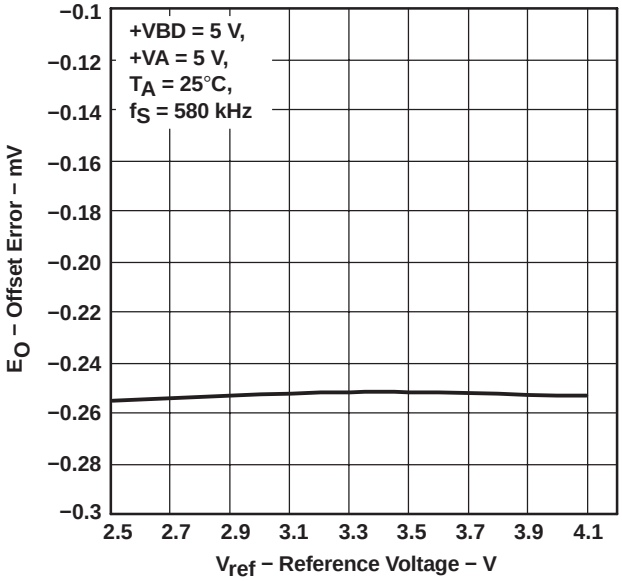



**Figure 30**

**SIGNAL-TO-NOISE RATIO**
**vs**
**FREE-AIR TEMPERATURE**

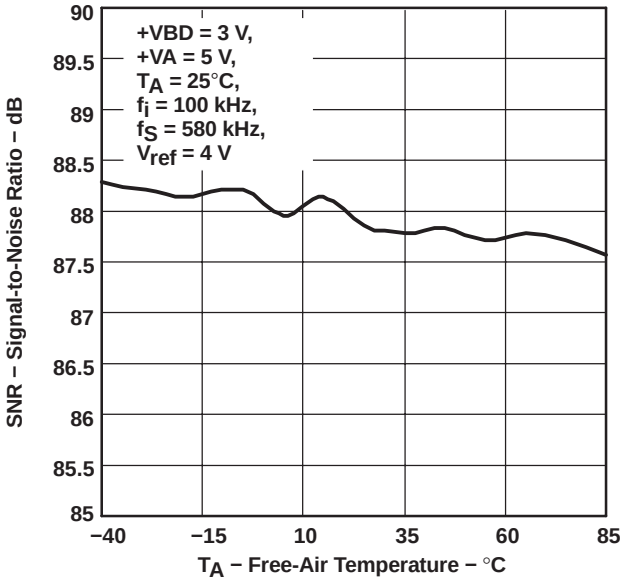



**Figure 31**

**TOTAL HARMONIC DISTORTION**
**vs**
**FREE-AIR TEMPERATURE**

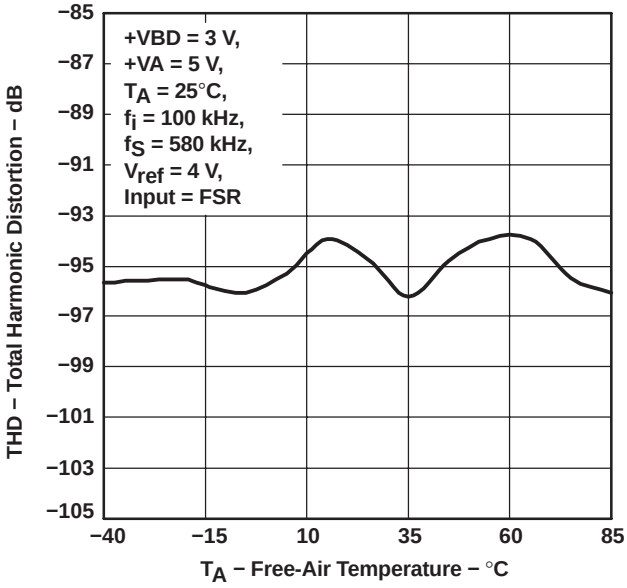



**Figure 32**

**SPURIOUS FREE DYNAMIC RANGE vs FREE-AIR TEMPERATURE**

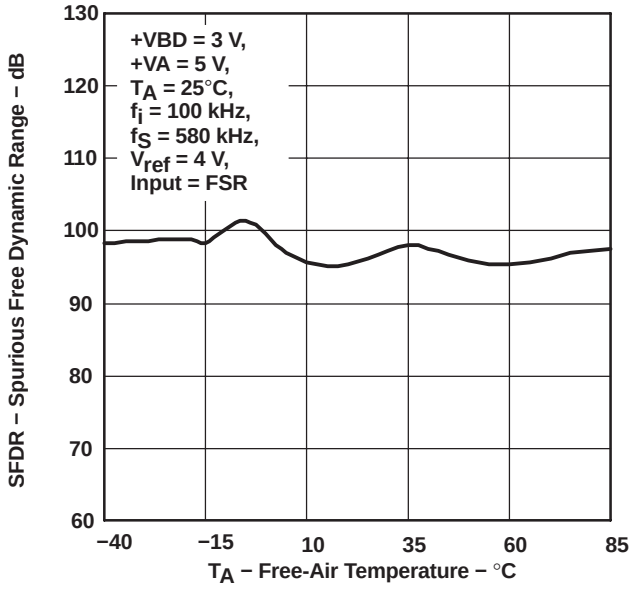



**Figure 33**

**SIGNAL-TO-NOISE AND DISTORTION vs FREE-AIR TEMPERATURE**

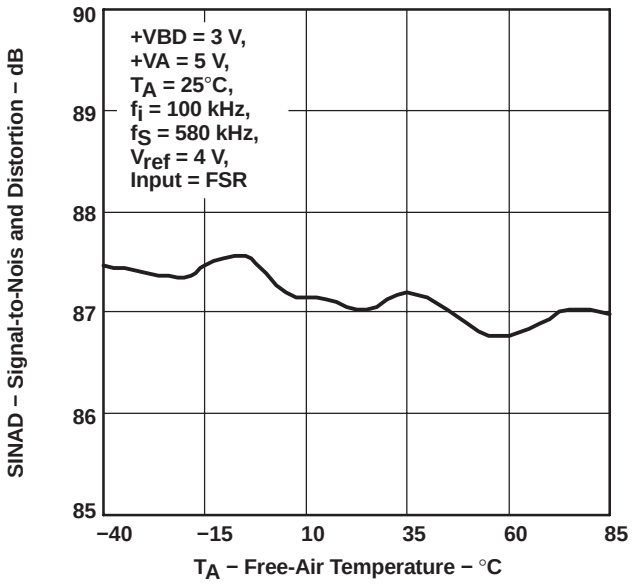



**Figure 34**

**EFFECTIVE NUMBER OF BITS vs FREE-AIR TEMPERATURE**

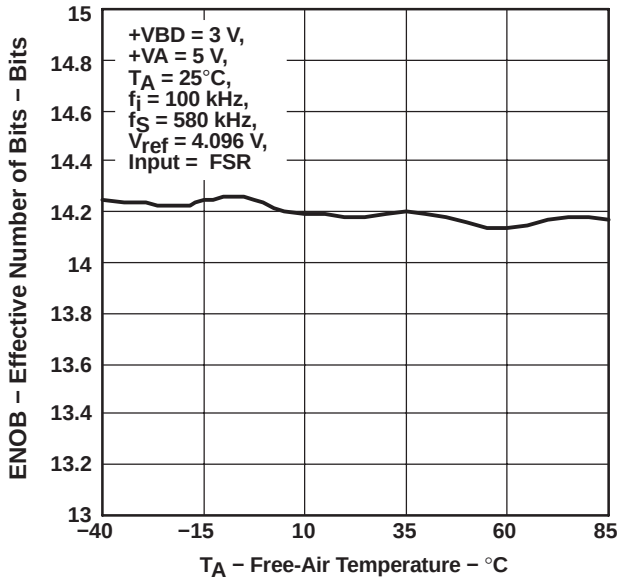



**Figure 35**

**SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY**

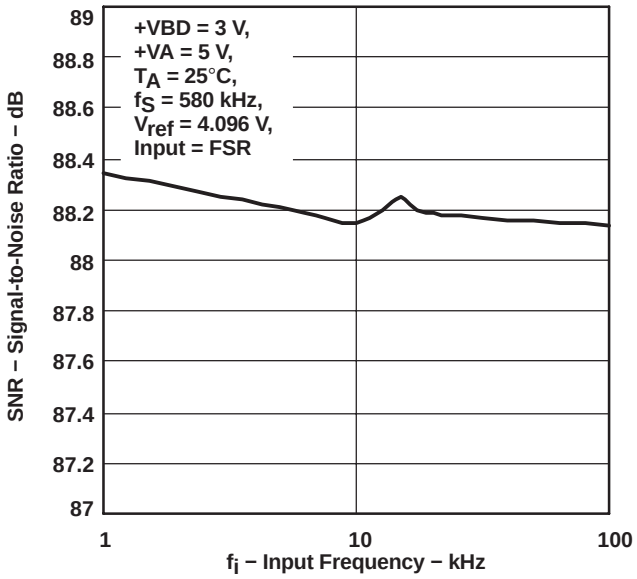



**Figure 36**

**TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY**

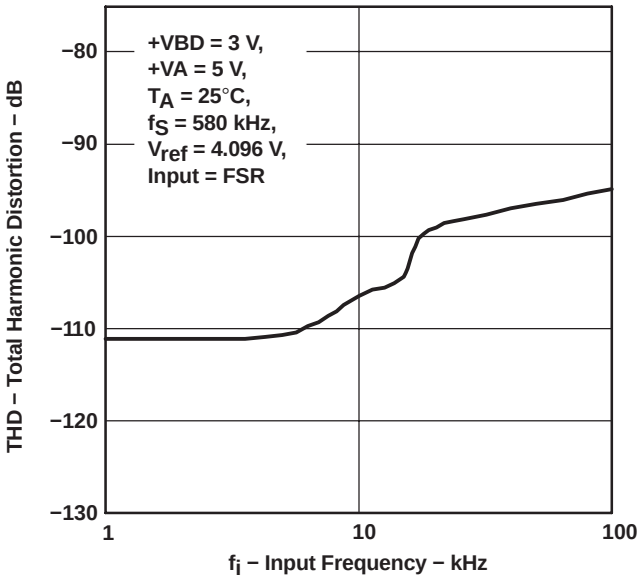



**Figure 37**

**SIGNAL-TO-NOISE AND DISTORTION vs INPUT FREQUENCY**

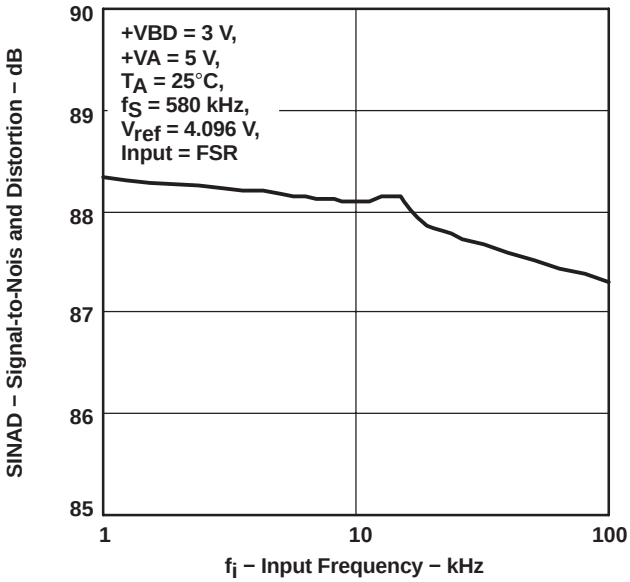



**Figure 38**

**EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY**

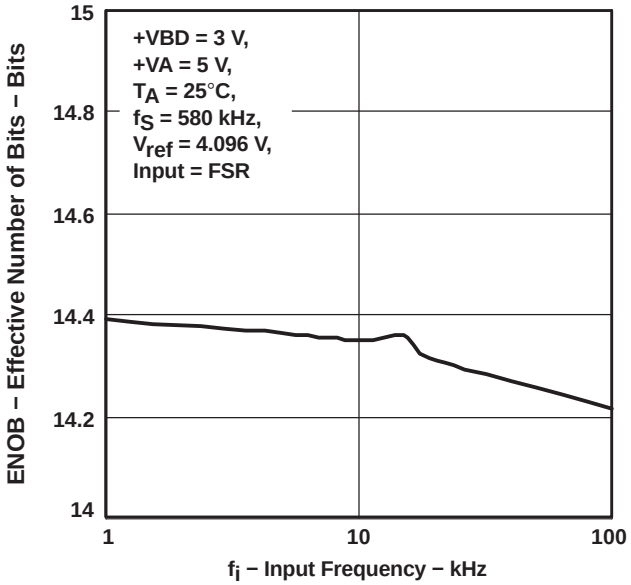



**Figure 39**

**SPURIOUS FREE DYNAMIC RANGE vs INPUT FREQUENCY**

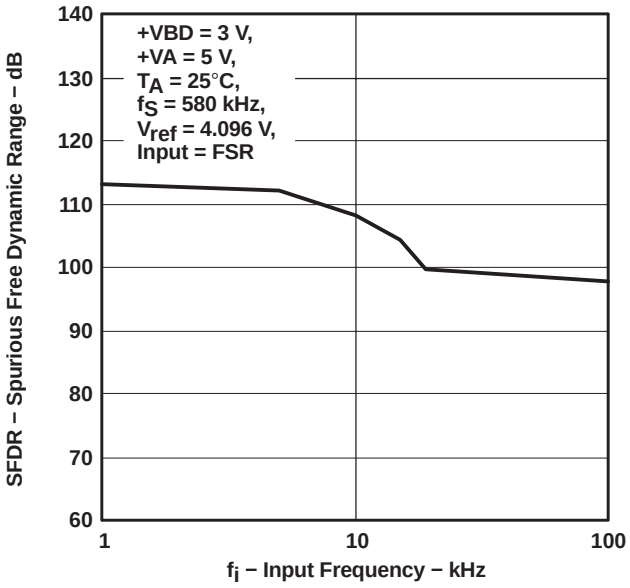



**Figure 40**

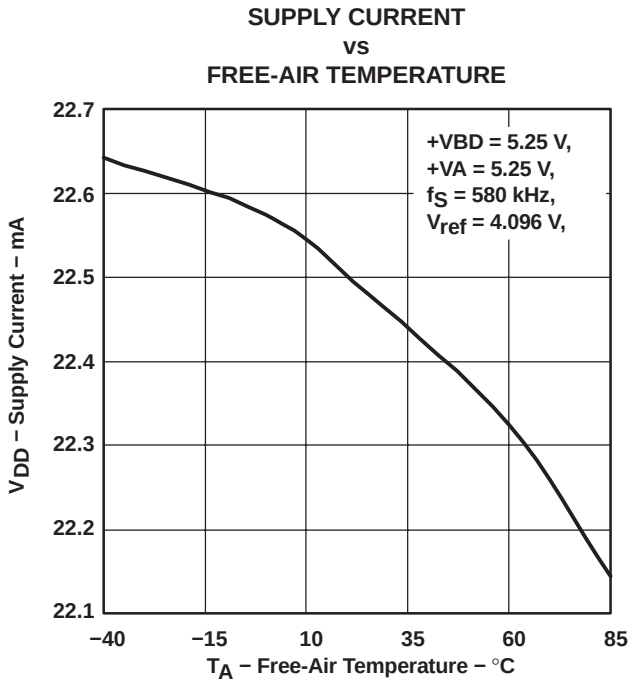



Figure 41

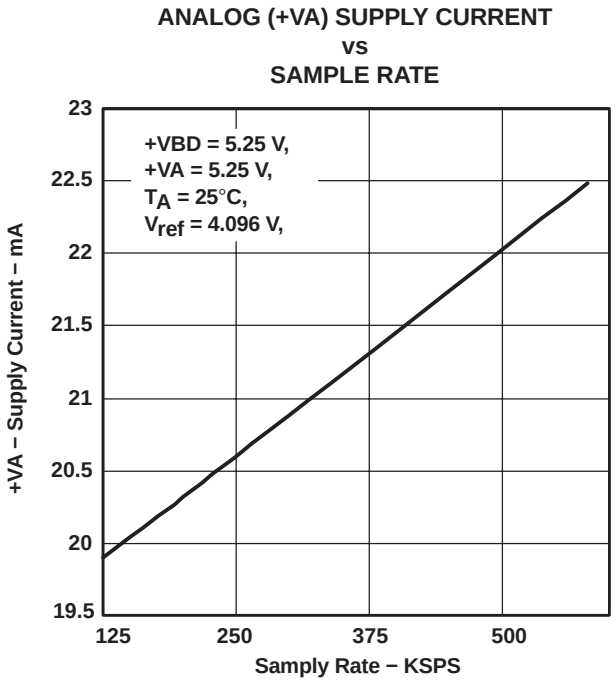



Figure 42

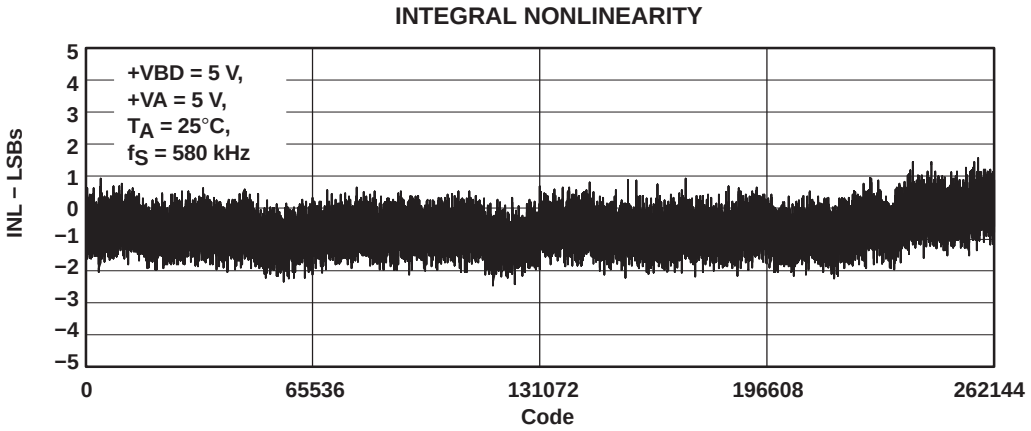



Figure 43

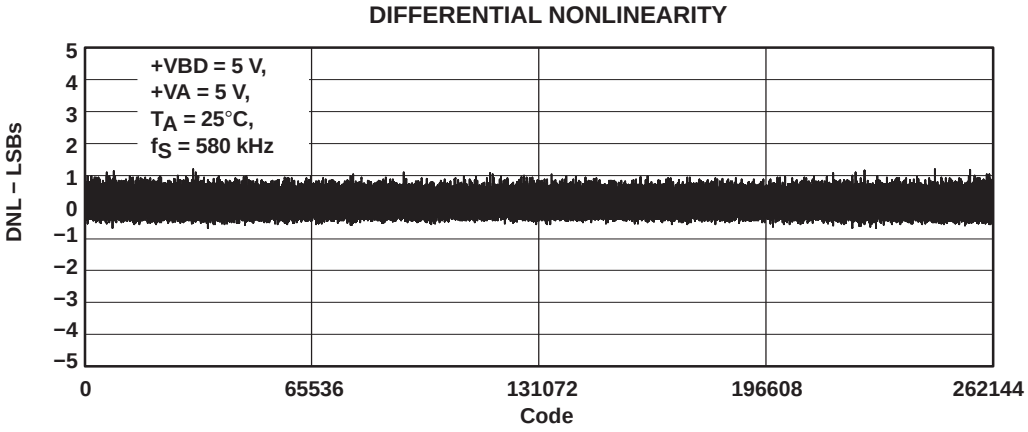



**Figure 44**

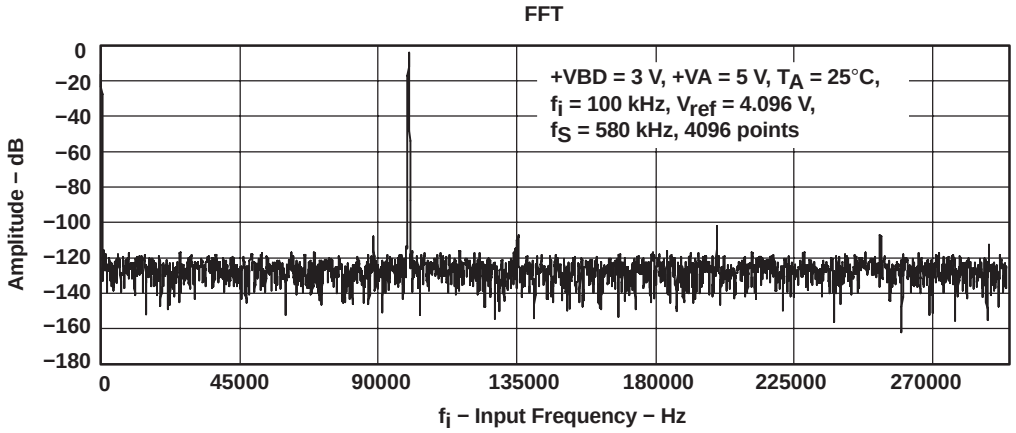



**Figure 45**

## APPLICATION INFORMATION

### MICROCONTROLLER INTERFACING

#### ADS8381 to 8-Bit Microcontroller Interface

Figure 46 shows a parallel interface between the ADS8381 and a typical microcontroller using the 8-bit data bus. The BUSY signal is used as a falling-edge interrupt to the microcontroller.

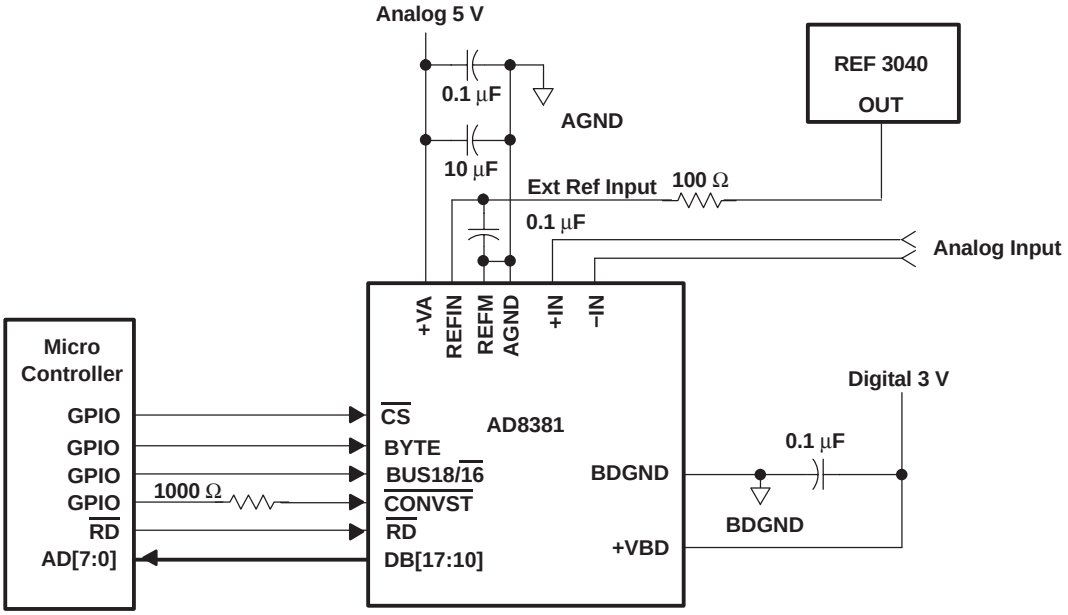



**Figure 46. ADS8381 Application Circuitry**

## PRINCIPLES OF OPERATION

The ADS8381 is a high-speed successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on charge redistribution which inherently includes a sample/hold function. See Figure 46 for the application circuit for the ADS8381.

The conversion clock is generated internally. The conversion time of 1.4 µs is capable of sustaining a 580-kHz throughput.

The analog input is provided to two input pins: +IN and −IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

## REFERENCE

The ADS8381 can operate with an external reference with a range from 2.5 V to 4.2 V. The reference voltage on the input pin 1 (REFIN) of the converter is internally buffered. A clean, low noise, well-decoupled reference voltage on this pin is required to ensure good performance of the converter. A low noise band-gap reference like the REF3040 can be used to drive this pin. A 0.1-uF decoupling capacitor is required between pin 1 and pin 48 of the converter. This capacitor should be placed as close as possible to the pins of the device. Designers should strive to minimize the routing length of the traces that connect the terminals of the capacitor to the pins of the converter. An RC network can also be used to filter the reference voltage. A 100-Ω series resistor and a 0.1-uF capacitor, which can also serve as the decoupling capacitor, can be used to filter the reference voltage.

## ANALOG INPUT

When the converter enters the hold mode, the voltage difference between the +IN and −IN inputs is captured on the internal capacitor array. The voltage on the −IN input is limited between –0.2 V and 0.2 V, allowing the input to reject small signals which are common to both the +IN and −IN inputs. The +IN input has a range of –0.2 V to $V_{ref}$ + 0.2 V. The input span (+IN − (−IN)) is limited to 0 V to $V_{ref}$.

The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8381 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (45 pF) to an 18-bit settling level within the acquisition time (300 ns) of the device. When the converter goes into the hold mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the +IN and −IN inputs and the span (+IN − (−IN)) should be within the limits specified. Outside of these ranges, the converter's linearity may not meet specifications. To minimize noise, low bandwidth input signals with low-pass filters should be used.

Care should be taken to ensure that the output impedance of the sources driving the +IN and −IN inputs are matched. If this is not observed, the two inputs could have different setting times. This may result in offset error, gain error, and linearity error which changes with temperature and input voltage.

The analog input to the converter needs to be driven with a low noise, high-speed op-amp like the THS4031. An RC filter is recommended at the input pins to low-pass filter the noise from the source. A series resistor of 15 Ω and a decoupling capacitor of 1.2 nF is recommended.

The input to the converter is a unipolar input voltage in the range 0 V to $V_{ref}$. The THS4031 can be used in the source follower configuration to drive the converter.

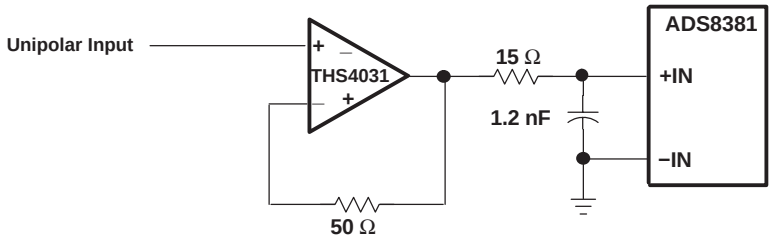



**Figure 47. Unipolar Input to Converter**

In systems where the input is bipolar, the THS4031 can be used in the inverting configuration with an additional DC bias applied to its + input so as to keep the input to the ADS8381 within its rated operating voltage range. This configuration is also recommended when the ADS8381 is used in signal processing applications where good SNR and THD performance is required. The DC bias can be derived from the REF3020 or the REF3040 reference voltage ICs. The input configuration shown below is capable of delivering better than 88-dB SNR and –95-db THD at an input frequency of 100 kHz. In case bandpass filters are used to filter the input, care should be taken to ensure that the signal swing at the input of the bandpass filter is small so as to keep the distortion introduced by the filter minimal. In such cases, the gain of the circuit shown in Figure 48 can be increased to keep the input to the ADS8381 large to keep the SNR of the system high. Note that the gain of the system from the + input to the output of the THS4031 in such a configuration is a function of the gain of the AC signal. A resistor divider can be used to scale the output of the REF3020 or REF3040 to reduce the voltage at the DC input to THS4031 to keep the voltage at the input of the converter within its rated operating range.

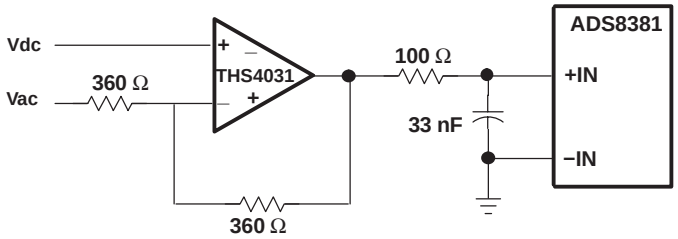



**Figure 48. Bipolar Input to Converter**

## DIGITAL INTERFACE

### Timing And Control

See the timing diagrams in the specifications section for detailed information on timing signals and their requirements.

The ADS8381 uses an internal oscillator generated clock which controls the conversion rate and in turn the throughput of the converter. No external clock input is required.

Conversions are initiated by bringing the $\overline{\text{CONVST}}$ pin low for a minimum of 40 ns (after the 40 ns minimum requirement has been met, the $\overline{\text{CONVST}}$ pin can be brought high), while $\overline{\text{CS}}$ is low. The BUSY output is brought high immediately following $\overline{\text{CONVST}}$ going low. BUSY stays high throughout the conversion process and returns low when the conversion has ended. Sampling starts with the falling edge of the BUSY signal when $\overline{\text{CS}}$ is tied low or starts with the falling edge of $\overline{\text{CS}}$ when BUSY is low.

Both $\overline{\text{RD}}$ and $\overline{\text{CS}}$ can be high during and before a conversion with one exception ($\overline{\text{CS}}$ must be low when $\overline{\text{CONVST}}$ goes low to initiate a conversion). Both the $\overline{\text{RD}}$ and $\overline{\text{CS}}$ pins are brought low in order to enable the parallel output bus with the conversion.

### Digital Inputs

The converter switches from sample to hold mode at the falling edge of the $\overline{\text{CONVST}}$ input pin. A clean and low jitter falling edge is important to the performance of the converter. A sharp falling transition on this pin can affect the voltage that is acquired by the converter. A falling transition time in the range of 10 ns to 30 ns is required to achieve the rated performance of the converter. A resistor of approximately 1000 Ω (10% tolerance) can be placed in series with the $\overline{\text{CONVST}}$ input pin to satisfy this requirement.

The other digital inputs to the ADS8381 do not require any resistors in series with them. However, certain precautions are necessary to ensure that transitions on these inputs do not affect converter performance. It is recommended that all activity on the input pins happen during the first 600 ns of the conversion period. This allows the error correction circuits inside the device to correct for any errors that these activities cause on the converter output. For example, when the converter is operated with $\overline{\text{CS}}$ and $\overline{\text{RD}}$ tied to ground, the signal $\overline{\text{CONVST}}$ can be brought low to initiate a conversion and brought high after a duration not exceeding 600 ns. Figure 49 shows the recommended timing for the $\overline{\text{CONVST}}$ input with $\overline{\text{RD}}$ and $\overline{\text{CS}}$ tied low.

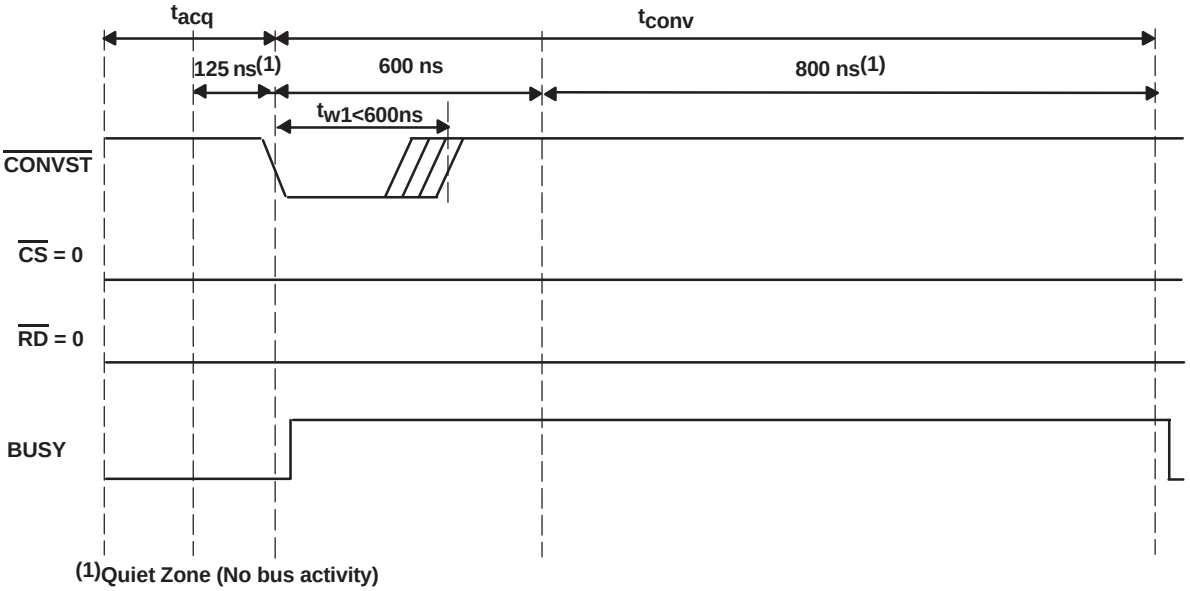



**Figure 49. Timing for $\overline{\text{CONVST}}$ When $\overline{\text{CS}}$ = $\overline{\text{RD}}$ = BDGND**

A similar precaution applies when $\overline{RD}$ is used to three-state the output buffers after a data-read operation. A minimum quite period of 125 ns is also required from the instant the data is changed on the bus (such as the falling or rising edge of $\overline{RD}$, the falling or rising edge of BYTE, and the falling or rising edge of BUS18/$\overline{16}$) is made available on the data bus pins to the sampling instant (falling edge of $\overline{CONVST}$). Figure 50 shows the timing of the input control signals that allow these conditions to be satisfied.

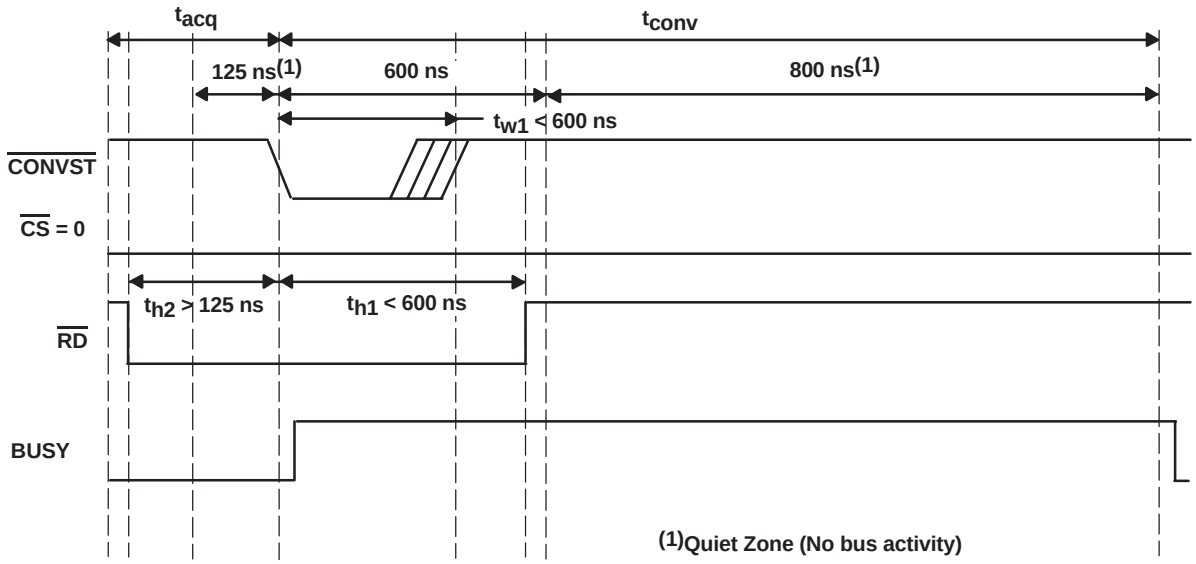



**Figure 50. Bus Activity Split to Avoid Quiet Zone**

If the $\overline{RD}$ pin is brought high to three-state the data buses, the three-stating operation should occur 125 ns before the end of the acquisition phase. Figure 51 shows the recommended timing for using the ADS8381 in this mode of operation. The same principle applies to other bus activities such as BYTE and BUS18/$\overline{16}$.

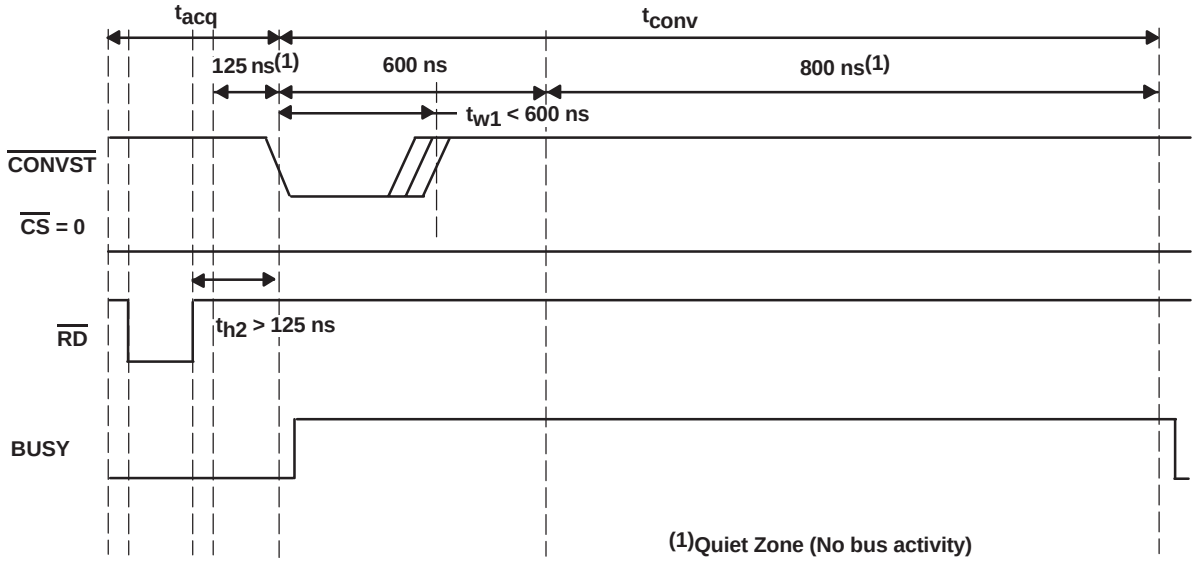



**Figure 51. Read Timing if the Bus Needs to be Three-Stated**

### Reading Data

The ADS8381 outputs full parallel data in straight binary format as shown in Table 1. The parallel output is active when $\overline{CS}$ and $\overline{RD}$ are both low. Any other combination of $\overline{CS}$ and $\overline{RD}$ sets the parallel output to 3-state. BYTE and BUS18/$\overline{16}$ are used for multiword read operations. BYTE is used whenever lower bits on the bus are output on the higher byte of the bus. BUS18/$\overline{16}$ is used whenever the last two bits on the 18-bit bus is output on either bytes of the higher 16-bit bus. Refer to Table 1 for ideal output codes.

**Table 1. Ideal Input Voltages and Output Codes**

| DESCRIPTION | ANALOG VALUE | DIGITAL OUTPUT STRAIGHT BINARY | |
|---|---|---|---|
| Full scale range | $(+V_{ref})$ | | |
| Least significant bit (LSB) | $(+V_{ref})/262144$ | BINARY CODE | HEX CODE |
| +Full scale | $(+V_{ref})$ – 1 LSB | 11 1111 1111 1111 1111 | 3FFFF |
| Midscale | $(+V_{ref})/2$ | 10 0000 0000 0000 0000 | 20000 |
| Midscale – 1 LSB | $(+V_{ref})/2$ – 1 LSB | 01 1111 1111 1111 1111 | 1FFFF |
| Zero | 0 V | 00 0000 0000 0000 0000 | 00000 |

The output data is a full 18-bit word (D17−D0) on DB17–DB0 pins (MSB−LSB) if both BUS18/$\overline{16}$ and BYTE are low.

The result may also be read on an 16-bit bus by using only pins DB17−DB2. In this case two reads are necessary: the first as before, leaving both BUS18/$\overline{16}$ and BYTE low and reading the 16 most significant bits (D17−D2) on pins DB17−DB2, then bringing BUS18/$\overline{16}$ high while holding BYTE low. When BUS18/$\overline{16}$ is high, the lower two bits (D1–D0) appear on pins DB3−DB2.

The result may also be read on an 8-bit bus for convenience. This is done by using only pins DB17−DB10. In this case three reads are necessary: the first as before, leaving both BUS18/$\overline{16}$ and BYTE low and reading the 8 most significant bits on pins DB17−DB10, then bringing BYTE high while holding BUS18/$\overline{16}$ low. When BYTE is high, the medium bits (D9−D2) appear on pins DB17−DB10. The last read is done by bringing BUS18/$\overline{16}$ high while holding BYTE high. When BUS18/$\overline{16}$ is high, the lower two bits (D1–D0) appear on pins DB11−DB10. The last read cycle is not necessary if only the first 16 most significant bits are of interest.

All of these multiword read operations can be performed with multiple active $\overline{RD}$ (toggling) or with $\overline{RD}$ held low for simplicity. This is referred to as the AUTO READ operation.

**Table 2. Conversion Data Read Out**

| BYTE | BUS18/$\overline{16}$ | DATA READ OUT | | | | |
|---|---|---|---|---|---|---|
| | | DB17−DB12 PINS | DB11−DB10 PINS | DB9−DB4 PINS | DB3−DB2 PINS | DB1−DB0 PINS |
| High | High | All One's | D1−D0 | All One's | All One's | All One's |
| Low | High | All One's | All One's | All One's | D1−D0 | All One's |
| High | Low | D9−D4 | D3−D2 | All One's | All One's | All One's |
| Low | Low | D17−D12 | D11−D10 | D9−D4 | D3−D2 | D1−D0 |

## RESET

The device can be reset through the use of the combination fo $\overline{CS}$ and $\overline{CONVST}$. Since the BUSY signal is held at high during the conversion, either one of these conditions triggers an internal self-clear reset to the converter.

- Issue a $\overline{CONVST}$ when $\overline{CS}$ is low and internal CONVERT state is high. The falling edge of $\overline{CONVST}$ starts a reset.
- Issue a $\overline{CS}$ (select the device) while internal CONVERT state is high. The falling edge of $\overline{CS}$ causes a reset.

Once the device is reset, all output latches are cleared (set to zeroes) and the BUSY signal is brought low. A new sampling period is started at the falling edge of the BUSY signal immediately after the instant of the internal reset.

## INITIALIZATION

At first power on there are three read cycles required ($\overline{RD}$ must be toggled three times). If conversion cycle is attempted before these initialization read cycles, the first three conversion cycles will not produce valid results. This is used to load factory trimming data for a specific device to assure high accuracy of the converter. Because of this requirement, the $\overline{RD}$ pin cannot be tied permanently to BDGND. System designers can still achieve the AUTO READ function if the power-on requirement is satisfied.

## LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8381 circuitry.

As the ADS8381 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are at least n *windows* in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event.

On average, the ADS8381 draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1-µF bypass capacitor is recommended from pin 1 (REFIN) directly to pin 48 (REFM). REFM and AGND should be shorted on the same ground plane under the device.

The AGND and BDGND pins should be connected to a clean ground point. In all cases, this should be the analog ground. Avoid connections which are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout consists of an analog ground plane dedicated to the converter and associated analog circuitry.

As with the AGND connections, +VA should be connected to a 5-V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. Power to the ADS8381 should be clean and well bypassed. A 0.1-µF ceramic bypass capacitor should be placed as close to the device as possible. See Table 3 for the placement of the capacitor. In addition, a 1-µF to 10-µF capacitor is recommended. In some situations, additional bypassing may be required, such as a 100-µF electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5-V supply, removing the high frequency noise.

**Table 3. Power Supply Decoupling Capacitor Placement**

| POWER SUPPLY PLANE | CONVERTER ANALOG SIDE | CONVERTER DIGITAL SIDE |
|---|---|---|
| SUPPLY PINS | | |
| Pin pairs that require shortest path to decoupling capacitors | (4,5), (8,9), (10,11), (13,15), (43,44), (45,46) | (24,25) |
| Pins that require no decoupling | 12, 14 | 37 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS8381IBPFBT | ACTIVE | TQFP | PFB | 48 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ADS8381I B | Samples |
| ADS8381IPFBT | NRND | TQFP | PFB | 48 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ADS8381I | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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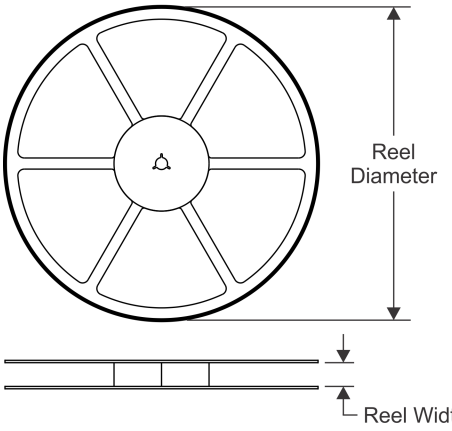
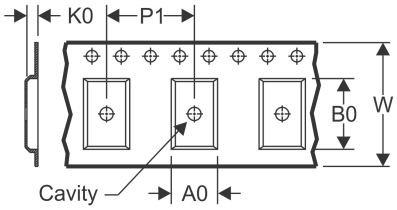
**REEL DIMENSIONS**

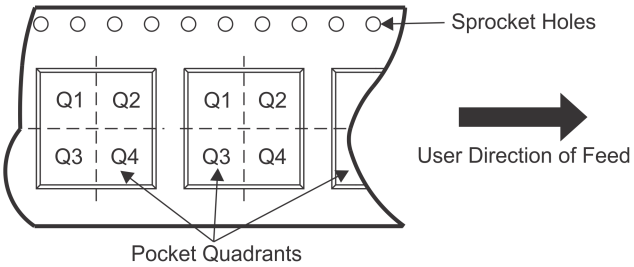



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

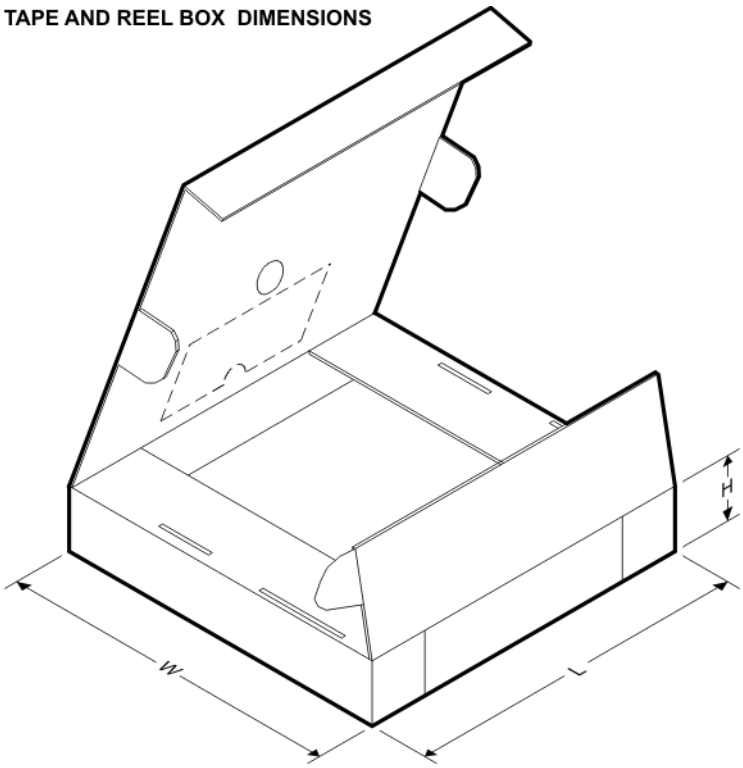
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS8381IBPFBT | TQFP | PFB | 48 | 250 | 180.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| ADS8381IPFBT | TQFP | PFB | 48 | 250 | 180.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |

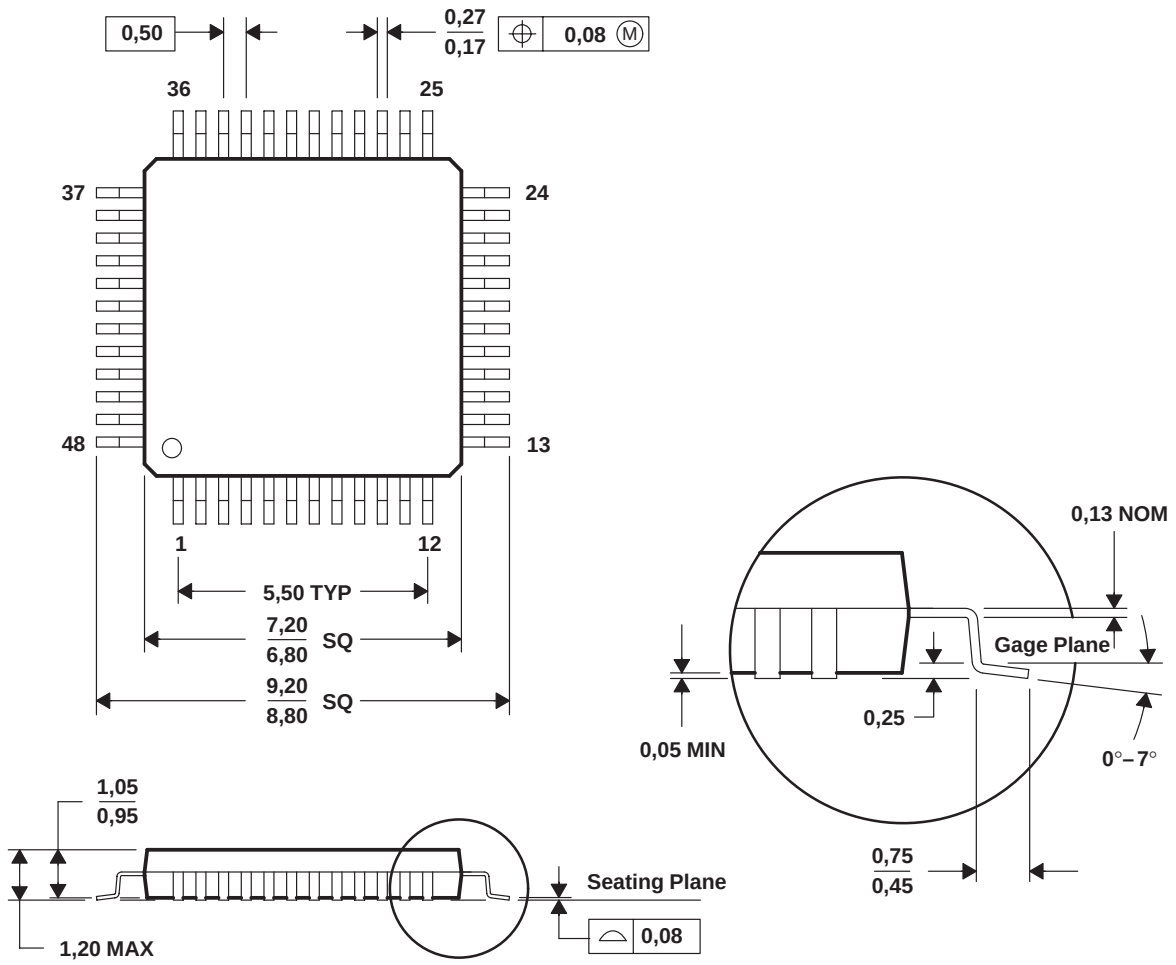
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

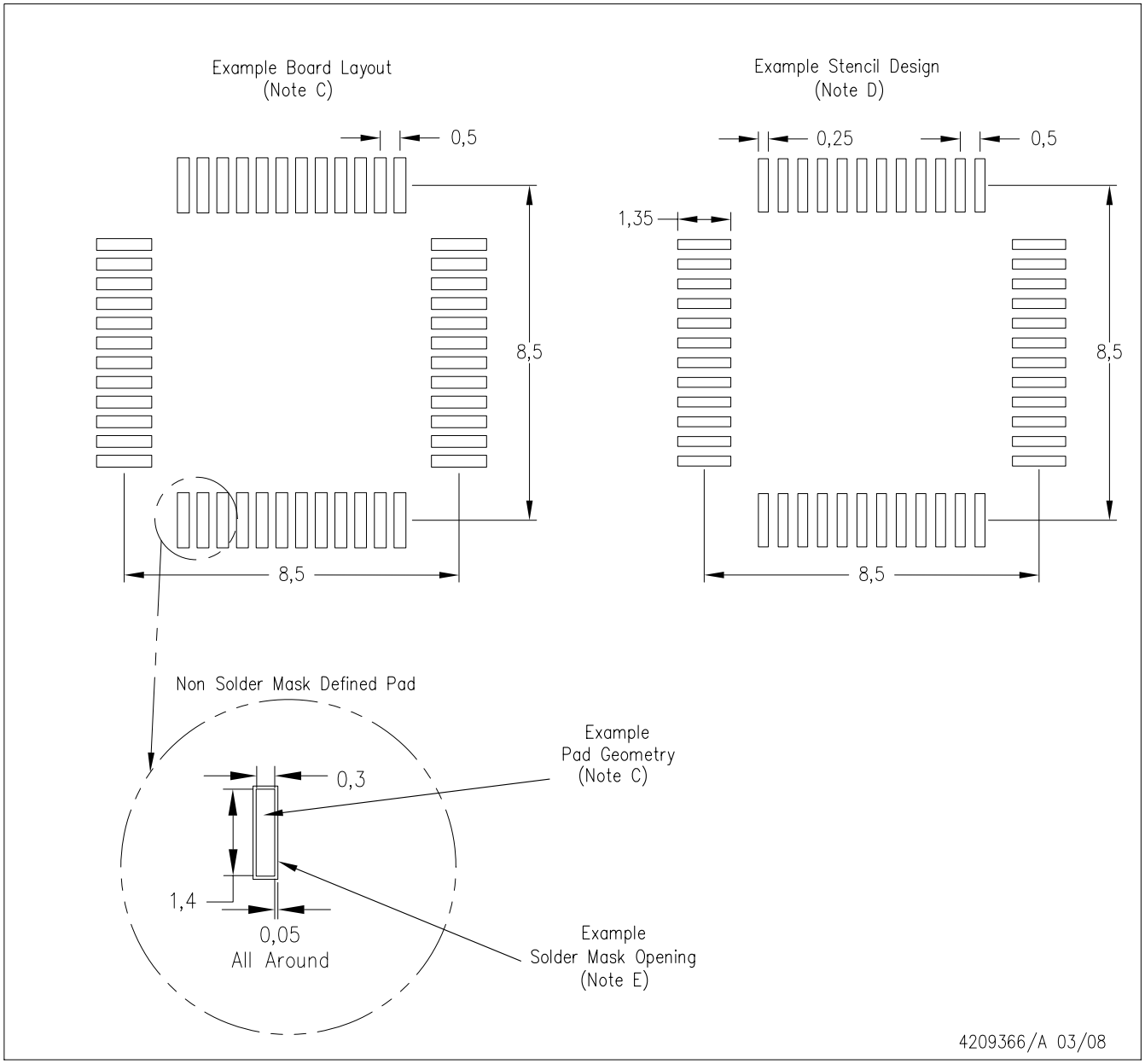
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADS8381IBPFBT | TQFP | PFB | 48 | 250 | 213.0 | 191.0 | 55.0 |
| ADS8381IPFBT | TQFP | PFB | 48 | 250 | 213.0 | 191.0 | 55.0 |

**PFB (S-PQFP-G48)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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